



## PRODUCT INFORMATION LETTER

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PIL IPD-IPC/13/7674  
Dated 28 Nov 2014

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**L7985x, L7986x : metal mask change**

Sales Type/product family label	see attached list
Type of change	Product design change
Reason for change	To improve the ESD robustness.
Description	Metal fix (from BA to BB version) in order to improve the CDM immunity level.
Forecasted date of implementation	21-Nov-2014
Forecasted date of samples for customer	21-Nov-2014
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	21-Nov-2014
Involved ST facilities	Catania, Ctm8

## DOCUMENT APPROVAL

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## ATTACHMENT TO PIL IPD-IPC/13/7674

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### **WHAT:**

We have introduced a silicon design change through a metal mask modification, on product line UA50, upgrading from BA to BB revision.

The impacted products are:

Commercial Products	Package	Packaging type
L7985TR	VFQFPN10	
L7986TR		
L7985ATR		Tape & Reel
L7986ATR		
L7986TATR		
L7985A	HSOP8	
L7986A		Tube
L7986TA		

### **WHY:**

To ensure a higher ESD robustness (CDM) compared to the standard qualification level.

### **HOW:**

The change from UA50BA5 to UA50BB5 consists of a metal mask change modification in order to improve the CDM level, from the  $\pm 300V$  on all pins, to the  $\pm 500V$  on all pins and  $\pm 750$  on corner pins.

### **WHEN:**

The metal mask change has already been evaluated on the automotive grade revision (UA50BBA, see Reliability Report RR003812CS2047) and is effective immediately.

Samples of the BB version are available upon request.

# Reliability Report

General Information		Locations	
Product Line	UA50 BBA	Wafer fab location	CATANIA M5
Product Description	Step-down switching regulator	Assembly plant location	AMKOR ATP1
Product division	I&PC	Reliability assessment	Pass
Package	HSOP8		
Silicon process technology	BCD6s 4M		

## DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	17-12-2012	13	G.D'Angelo	Original document

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## 1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

## 2 RELIABILITY EVALUATION OVERVIEW

### 2.1 Objectives

This report contains the reliability evaluation performed on the UA50 BBA device diffused in CATANIA M5 and assembled in HSOP8 in AMKOR ATP1, according to the AEC-Q100 (Grade1) specifications.

Considering that the device is a derivative of the full qualified U50 BAA device (see RR004611CS2047), a reduced set of trials has been performed according to the AEC-Q100 (Grade1) specifications.

Below is the list of the trials performed:

#### Die Oriented Tests

- Power Temperature Cycling

#### Package Oriented Tests

- Preconditioning
- Temperature Cycling

#### Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

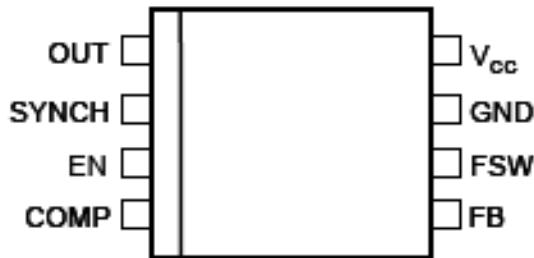
### 2.2 Conclusion

Taking in account the results of the trials performed the UA50 BBA diffused in CATANIA M5 and assembled in HSOP8 in AMKOR ATP1 can be qualified for automotive applications from reliability viewpoint.

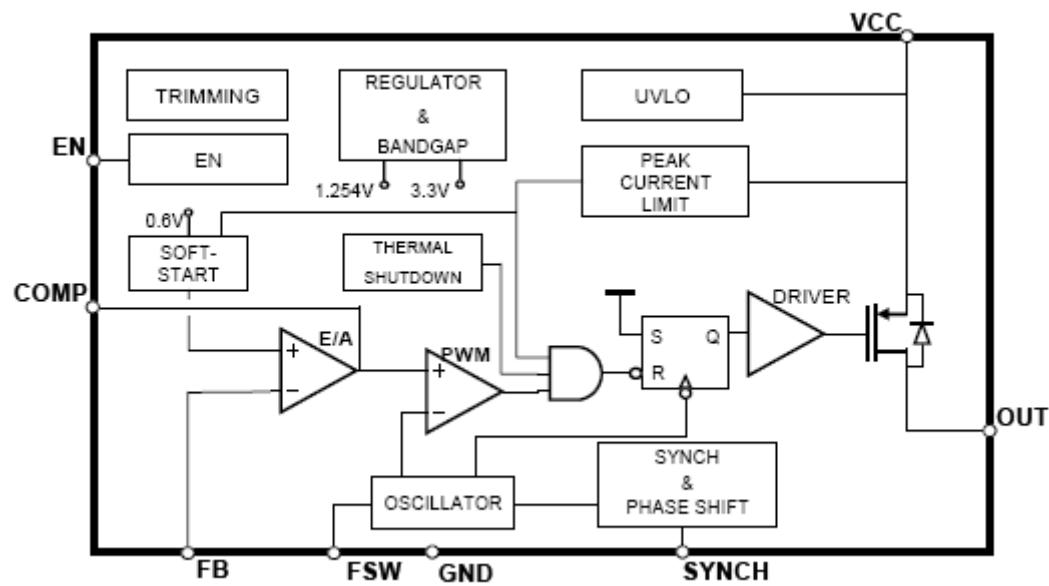
### 3 DEVICE CHARACTERISTICS

#### 3.1 Device description

##### 3.1.1 Pin connection (top view)



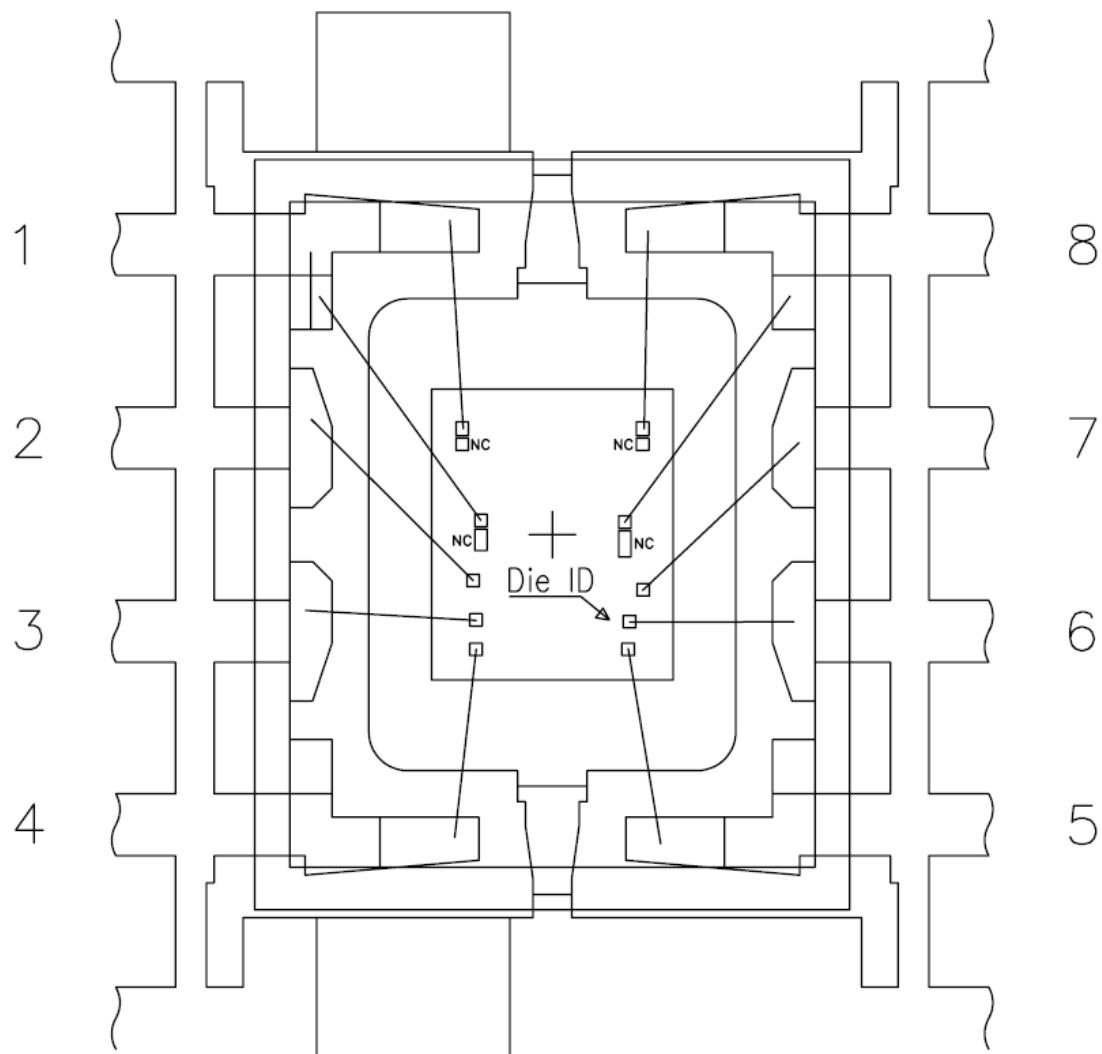
### 3.1.2 Block diagram



### 3.1.3 Bonding diagram

FRAME PAD :  $\frac{.095 \times .122 \text{ inch}}{2.413 \times 3.099 \text{ mm}}$

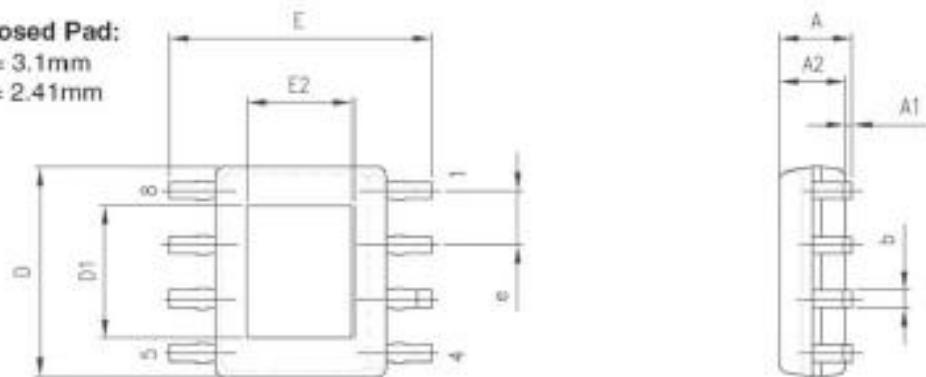
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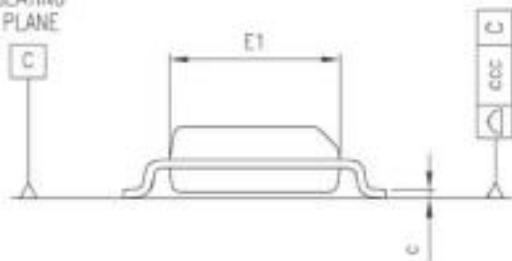
### 3.1.4 Package outline/Mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.70			0.0669
A1	0.00		0.15		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
E	5.80	6.00	6.20	0.2283		0.2441
E1	3.80	3.90	4.00	0.1496		0.1575
e		1.27				
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0		8			0.3150
ccc			0.10			0.0039

Exposed Pad:  
 D1 = 3.1mm  
 E2 = 2.41mm



SEATING  
PLANE



## Traceability

Wafer fab information	
<b>Wafer fab manufacturing location</b>	CATANIA M5
<b>Wafer diameter</b>	8 inches
<b>Wafer thickness</b>	375µm
<b>Silicon process technology</b>	BCD6s 4M
<b>Die finishing back side</b>	Cr/Ni/Au
<b>Die size</b>	1909x1587µm
<b>Bond pad metallization layers</b>	Al/Cu
<b>Passivation</b>	USG+SiN+Polyimide
<b>Metal levels</b>	4

Assembly Information	
<b>Assembly plant location</b>	AMKOR ATP1
<b>Package Description</b>	HSOP8
<b>Molding compound</b>	G600
<b>Wires bonding materials/diameters</b>	Au/1.2mils
<b>Die attach material</b>	8290
<b>Lead solder material</b>	Sn

## 4 TESTS RESULTS SUMMARY

### 4.1 Test plan and results summary

Die Oriented Tests						
Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results
PTC	Power Temperature Cycling					
	On Chip Boards	T <sub>j</sub> =-40°C÷150°C V <sub>cc</sub> =25V, I <sub>out</sub> =0.7A	45	1	1000h	PASSED

Package Oriented Tests						
Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results
PC	Pre-Conditioning: Moisture sensitivity level 3					
		24h bake@125°C, 192h@30°C/60%R.H., Reflow Simulation (3times)	77	1		PASSED
TC	Temperature Cycling					
	PC before	-50°C/150°C in air	77	1	1000cy	PASSED

Electrical Characterization Tests						
Test	Method	Conditions	Sample/ Lots	Number of lots	Duration	Results
ESD	Electro Static Discharge					
	Human Body Model	+/- 2kV	3	1		PASSED
	Charge Device Model	+/- 500V +/- 750V on corner pins	3	1		PASSED
LU	Latch-Up					
	Over-voltage and Current Injection	T <sub>amb</sub> =125°C Jedec78	6	1		PASSED

## **5 TESTS DESCRIPTION & DETAILED RESULTS**

### **5.1 Die oriented tests**

#### **5.1.1 Power Temperature Cycling**

This test simulates typical power automotive application. The test is addressed mainly to focus die-attach and wire bonding problems in all the temperature stress changes.

Combined stress performing an HTOL stress while the ambient temperature is cycling between  $-40$  to  $+85^{\circ}\text{C}$  ( $T_j=150^{\circ}\text{C}$ ) with the DUT switched alternatively ON/OFF (5'each) in asynchronous mode with respect the ambient temperature change, (1 cycle: 10' @ stress Temp. / 20' to change Temperature).

The Test Duration is 1000h

The read-outs flow chart is the following:

- Initial testing @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$
- Check at 168 and 500hrs @  $T_a=25^{\circ}\text{C}$
- Final Testing (1000 hr.) @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$

## **5.2 Package oriented tests**

### **5.2.1 Pre-Conditioning**

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.

The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

The read-outs flow chart is the following:

- Initial testing @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$ .
- Final Testing @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$ .

### **5.2.2 Thermal Cycles**

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

The read-outs flow chart is the following:

- Initial testing @  $T_a=125^{\circ}\text{C}$ .
- Check at @ 500 cycles @  $T_a=25^{\circ}\text{C}$
- Final Testing @ 1000 cycles @  $T_a=125^{\circ}\text{C}$ .

#### TEST CONDITIONS:

- $T_a= -50^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ (air)
- 15 min. at temperature extremes
- 1 min. transfer time

## 5.3 Electrical Characterization Tests

### 5.3.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.

The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

### Stress applied setup 1 – Enable low:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
<i>IN</i> low: 0V	-10mA	I <sub>nom</sub> +100mA	V <sub>cc</sub> =44V
<i>IN</i> high: 3.3V	-10mA	I <sub>nom</sub> +100mA	V <sub>cc</sub> =44V

PIN 1, 4, 6 not perform trial

PIN 3 (EN) set LOW - tested only during negative trials

PIN 5 (EN) set LOW ,  
PIN 5 (FB) set to 1.2V

### Stress applied setup 2 – Enable high:

Stress applied setup 2 - Enable high:			
condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
<i>IN high: 3.3V</i>	-10mA	I <sub>nom</sub> +100mA	V <sub>cc</sub> =44V

PIN 3 (EN) set HIGH (not tested)

PIN 3 (EN) set HIGH (not test)

PIN 1, 4, 5, 6 hot

The read-outs flow chart is the following:

- Initial testing @  $T_a=25^\circ\text{C}/125^\circ\text{C}$
- Latch-UP trial @  $T_a=125^\circ\text{C}$
- Final Testing @  $T_a=25^\circ\text{C}/125^\circ\text{C}$

### 5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.

The read-outs flow chart is the following:

- Initial testing @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$
- ESD discharging @  $T_a=25^{\circ}\text{C}$
- Final Testing @  $T_a=25^{\circ}\text{C}/125^{\circ}\text{C}$

## TEST CONDITIONS:



## Public Products List

PIL Title : L7985x, L7986x : metal mask change

PIL Reference : IPD-IPC/13/7674

PIL Created on : 01-DEC-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

### ST COMMERCIAL PRODUCT

L7985A	L7985ATR
L7986A	L7986ATR
L7986TATR	L7986TR

L7985TR
L7986TA

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