



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/12/7438

Dated 24 Aug 2012

M95128, 128 Kbit SPI Bus EEPROM / Industrial range
Redesign and upgrade to the CMOSF8H process technology

Table 1. Change Implementation Schedule

Forecasted implementation date for change	17-Aug-2012
Forecasted availability date of samples for customer	17-Aug-2012
Forecasted date for STMicroelectronics change Qualification Plan results availability	17-Aug-2012
Estimated date of changed product first shipment	23-Nov-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M95128 products family
Type of change	Waferfab technology change
Reason for change	Line up to state-of-the-art of design
Description of the change	Redesign and upgrade to the new CMOSF8H Process technology
Change Product Identification	Process Technology identifier "K" for F8H
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

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Customer Acknowledgement of Receipt		PCN MMS-MMY/12/7438	
Please sign and return to STMicroelectronics Sales Office		Dated 24 Aug 2012	
☐ Qualification Plan Denied	Name:		
☐ Qualification Plan Approved	Title:		
	Company:		
☐ Change Denied	Date:		
☐ Change Approved	Signature:		
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DOCUMENT APPROVAL

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M95128, 128 Kbit SPI Bus EEPROM / Industrial range Redesign and upgrade to the CMOSF8H process technology

What is the change?

The **M95128**, 128 Kbit SPI bus EEPROM product's family, currently produced using the CMOSF8L process technology at ST Rousset (France) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H** process technology at the same wafer diffusion plant.

This upgraded version in CMOSF8H offers:

- **1.7 V / 5.5 V** ("DF") Vcc range
- Additional **Lockable Identification Page** ("-D").
- Frequency up to **20 MHz**
- Write cycles up to **4 millions**
- Data retention up to **200 years**

The new M95128 in CMOSF8H version is functionally compatible to the current CMOSF8L version, as per datasheet rev. 14 - January 2012, here attached.

The following parameters are updated in the revised datasheet (rev. 15):

Maximum Clock frequency:

- 20 MHz at Vcc > 4.5 V (*5 MHz for CMOSF8L version*)
- 10 MHz at Vcc > 2.5 V (*5 MHz for CMOSF8L version*)
- 5 MHz at Vcc > 1.8 V (*2 MHz for CMOSF8L version*)

Standby current:

- 3 µA at Vcc = 5.5 V (*5 µA for CMOSF8L version*)
- 2 µA at Vcc = 2.5 V (*5 µA for CMOSF8L version*)
- 1 µA at Vcc = 1.8 V (*3 µA for CMOSF8L version*)

Concurrent to this change, the following production rationalization will follow:

- SO8N (Narrow, 150 mils) assembled on SHD line at ST Shenzhen will use 0.8 mil Copper wire (as introduced in PCN MMS-MMY/11/6929).
- MLP 2x3 (UFDFPN) will change from small exposed pad (package code "MB") to large exposed pad (package code "MC"), PTN will be released in 2h/2012.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M95128 in the new CMOSF8H process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded M95128 with the new CMOSF8H will ramp up from September 2012 and shipments can start from middle of November 2012 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the M95128 was qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The CMOSF8H process technology is already qualified for this product family.

The intermediate **Qualification Report QRMMY1203** is available and included inside this document.

What is the impact of the change?

- **Form:** Marking change (see **Device marking** paragraph)
- **Fit:** Die dimension change
- **Function:**
 - change on **DC characteristics** (updated in datasheet rev. 15)
 - change on **AC performances** (updated in datasheet rev. 15)

How can the change be seen?

- **BOX LABEL MARKING**

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is “K” for the **upgraded version** in CMOSF8H, this identifier being “A” for the current version in CMOSF8L.

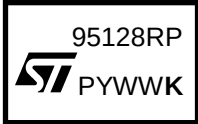
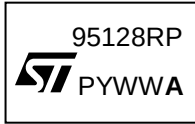
→ Example for M95128-BRMN6TP

STMicronics	Manufactured under patents or patents pending		
	Country Of Origin: XXXX		
	Pb-free	2 nd Level Interconnect	
	MSL: 1	NOT MOISTURE SENSITIVE	
	PBT: 260 °C Category: e4 ECOPACK2/ROHS		
	TYPE: M95128-RMN6TP		
	M95128-RMN6TPK X X		
	Total Qty:	2500	
	Process Technology: “K” for CMOSF8H “A” for CMOSF8L Mask revision and/or Wafer diffusion plant Assembly and Test & Finishing plants		
	Trace Codes	PPYWLLLL WX TF	
Marking	95128RP		
Bulk ID	X0X00XXX0000		
			
Please provide the bulk ID for any inquiry			

How can the change be seen?

- DEVICE MARKING

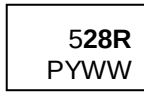
For the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit “T” for **process technology** identifier is “K” for the **upgraded version** in **CMOSF8H**, this identifier being “A” for the current version in CMOSF8L:

	Upgraded M95128 CMOSF8H	Current M95128 CMOSF8L
SO8N Example: M95128-RMN6TP		

For the TSSOP8 package, the difference is visible inside the product name where the last digit is “K” for the **upgraded version** in **CMOSF8H**, this identifier being “P” for the current version in CMOSF8L:

	Upgraded M95128 CMOSF8H	Current M95128 CMOSF8L
TSSOP8 Example: M95128-RDW6TP		

For the MLP8 package, the product name is “5GRK” for the **upgraded version** in **CMOSF8H**, while the current version in CMOSF8L is “528R”:

	Upgraded M95128 CMOSF8H	Current M95128 CMOSF8L
MLP8 2x3 Example: M95128-RMC6TG		

P = Assembly plant / country
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process technology code/ Wafer Fab ID

Appendix A- Product Change Information

Product family / Commercial products:	M95128 products family
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of design
Description of the change:	Redesign and upgrade to the new CMOSF8H Process technology.
Forecast date of the change: (Notification to customer)	Week 33 / 2012
Forecast date of <u>Qualification samples</u> availability for customer(s):	See details on next page
Forecast date for the internal STMicroelectronics change, <u>Qualification Report</u> availability:	The intermediate Qualification Report QRMMY1203 is available and included inside this document.
Marking to identify the changed product:	Process Technology identifier “ K ” for F8H
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 47 / 2012

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M95128-RMN6P (*)	SO8N	No sample in tube
M95128-RMN6TP (*)	SO8N	Available
M95128-WMN6P	SO8N	No sample in tube
M95128-WMN6TP	SO8N	Available
M95128-RDW6TP	TSSOP8	Available
M95128-RMC6TG	MLP8 2x3	Available

(*) Following product line rationalization, we recommend customer to use **-R** version (1.8 V – 5.5 V) when **-W** (2.5 V – 5.5 V) is used.

For instance, **M95128-RMN6TP should be preferred** to M95128-WMN6TP.

- The following part number will not be kept in production, replacement part number is:

Current Commercial Part Numbers	Replacement Commercial Part Numbers	Package	Samples availability
M95128-RMB6TG	M95128-RMC6TG	MLP8 2x3	Available

Appendix C: Qualification Report:

See following pages



QRMMY1203

Qualification report

New design / M95128-R M95128-W M95128-DF
using the CMOSF8H technology in the Rousset 8" Fab

Table 1. Product information

General information	
Commercial product	M95128-RMN6P M95128-RMN6TP M95128-RDW6TP M95128-RMC6TG M95128-WMN6TP M95128-WMN6P M95128-DFMN6TP M95128-DFDW6TP M95128-DFMC6TG M95128-DFCS6TP/K
Product description	128 Kbit serial SPI bus EEPROM with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8", France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
WLCSP	Subcon Stats ChipPac, Singapore	Subcon Stats ChipPac, Singapore

Reliability assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M95128 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for -W devices
- 1.8 to 5.5 V at –40 to 85 °C for -R devices
- 1.7 to 5.5 V at –40 to 85 °C for -DF devices

The CMOSF8H is a new advanced silicon process technology that is already qualified in the STMicroelectronics Rousset 8" diffusion plant, and is in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24128, M24C64/M95640 and M24C32/M95320 EEPROM products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The new design M95128 using the CMOSF8H silicon process technology in the ST Rousset 8" diffusion fab has passed all reliability requirements.

Refer to [Section 3: Reliability test results](#) for details on the test results.

2 Device characteristics

Device description

The M95128-R, M95128-W and M95128-DF are electrically erasable programmable memory (EEPROM) devices. They are accessed by a high speed SPI compatible bus. Their memory array is organized as 16 Kb × 8 bits.

The M95128-DF also offers an additional page, named the Identification Page (64 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as the Identification Page can be used to store unique identification parameters and/or parameters specific to the production line.

The device is accessed by a simple serial interface that is SPI-compatible.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in [Table 3](#).

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95128	CMOSF8H	ST Rousset 8"	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicles used for package qualification are presented in [Table 4](#).

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95M02 ⁽¹⁾	CMOSF8H	ST Rousset 8"	SO8N	ST Shenzhen / Subcon Amkor
M24M01 ⁽²⁾	CMOSF8H	ST Rousset 8"	TSSOP8	ST Shenzhen / Subcon Amkor
M24C64 / M24512	CMOSF8H	ST Rousset 8"	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / Subcon Amkor
M95M02 / M24512	CMOSF8H	ST Rousset 8"	WLCSP	Subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable to M95128.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable to M95128.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in [Table 5](#) for die-oriented tests
- in [Table 6](#) for SO8N ST Shenzhen package-oriented tests
- in [Table 7](#) for TSSOP8 ST Shenzhen package-oriented tests
- in [Table 8](#) for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests
- Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)⁽¹⁾

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size
						M95128
						Lot 1
EDR	High temperature operating life after endurance					
	AEC-Q100-005	400 000 E/W cycles at 150 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80
	Data retention after endurance					
	AEC-Q100-005	400 000 E/W cycles at 150 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80
LTOL	Low temperature operating life					
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80
HTSL	High temperature storage life					
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80
WEB	Program/erase endurance cycling + bake					
	Internal spec.	5 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	5 Million cycles / 48 hrs	0/80 ⁽²⁾
ESD HBM	Electrostatic discharge (human body model)					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)					
	AEC-Q100-004 JESD78	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A

1. See [Table 9: List of terms](#) for a definition of abbreviations.

2. First rejects after 10 million cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) ⁽¹⁾

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95M02 ⁽²⁾			M95128
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	−65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	−55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See [Table 9: List of terms](#) for a definition of abbreviations.

2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable to M95128.

3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) ⁽¹⁾

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24M01 ⁽²⁾			M95128
	Lot1	Lot2	Lot3	Lot4					
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	400	3	N/A	0/400	0/400	0/400	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	−65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	−55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See [Table 9: List of terms](#) for a definition of abbreviations.

2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable to M95128.

3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 (MLP8) 2 x 3 mm / ST Calamba) ⁽¹⁾

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C64 / M24512			M95128
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (2)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (2)	Temperature cycling								
	AEC-Q100-JESD22-A104	−65 °C / +150 °C	80	3	1000 cycles	0/80	0/80	0/80	-
			800	3	200 cycles	0/800	0/800	0/800	-
TMSK (2)	Thermal shocks								
	JESD22-A106	−55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (2)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (2)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field-induced charging method	18	1	N/A	Pass >1500 V	-	-	Results FC W35

1. See [Table 9: List of terms](#) for a definition of abbreviations.

2. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Aug-2012	1	Initial release.

Document Revision History		
Date	Rev.	Description of the Revision
August 07, 2012	1.00	First draft creation

Source Documents & Reference Documents		
Source document Title	Rev.:	Date:

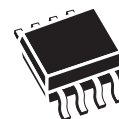


M95128 M95128-W M95128-R

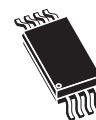
128 Kbit serial SPI bus EEPROM
with high speed clock

Features

- Compatible with SPI bus serial interface (positive clock SPI modes)
- Single supply voltage:
 - 4.5 to 5.5 V for M95128
 - 2.5 to 5.5 V for M95128-W
 - 1.8 to 5.5 V for M95128-R
- High speed
 - 10 MHz clock rate, 5 ms write time
- Status Register
- Hardware protection of the Status Register
- Byte and Page Write (up to 64 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD protection
- More than 1 000 000 write cycles
- More than 40-year data retention
- Packages
 - ECOPACK2® (RoHS compliant and Halogen-free)



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



UFDFPN8 (MB, MC)
2 × 3 mm (MLP)

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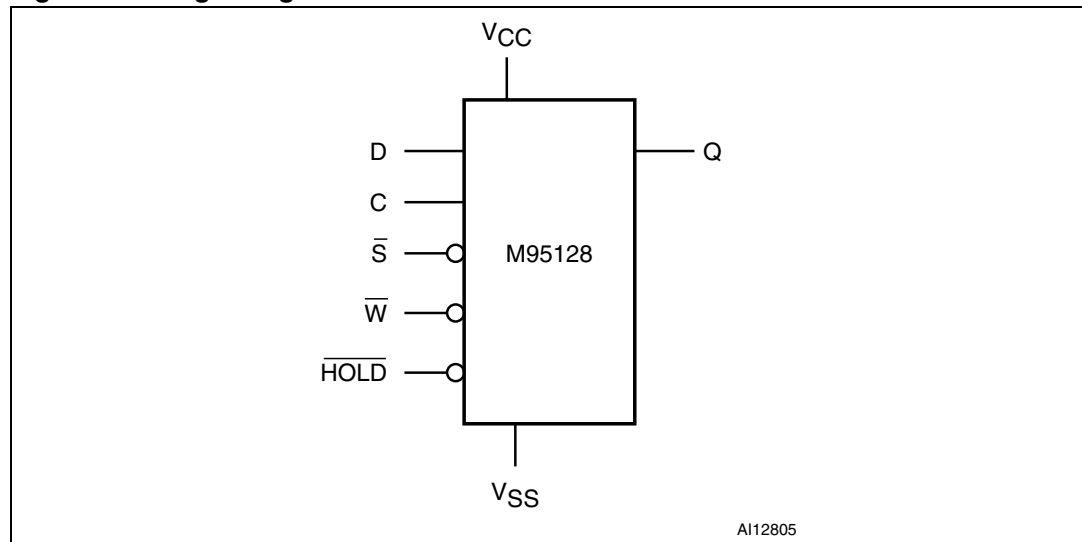
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1 Description

The M95128, M95128-W and M95128-R are electrically erasable programmable memory (EEPROM) devices accessed by a high speed SPI-compatible bus. The memory array is organized as 16384×8 bits.

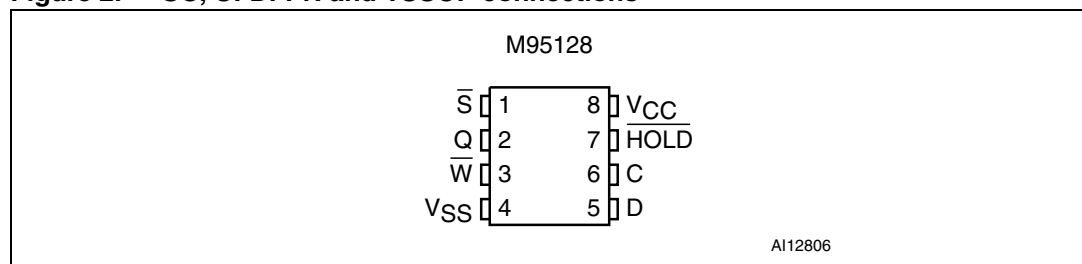
Figure 1. Logic diagram



The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in [Table 1](#) and [Figure 1](#).

The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Figure 2. SO, UFDFPN and TSSOP connections



1. See [Section 10: Package mechanical data](#) for package dimensions, and how to identify pin-1.

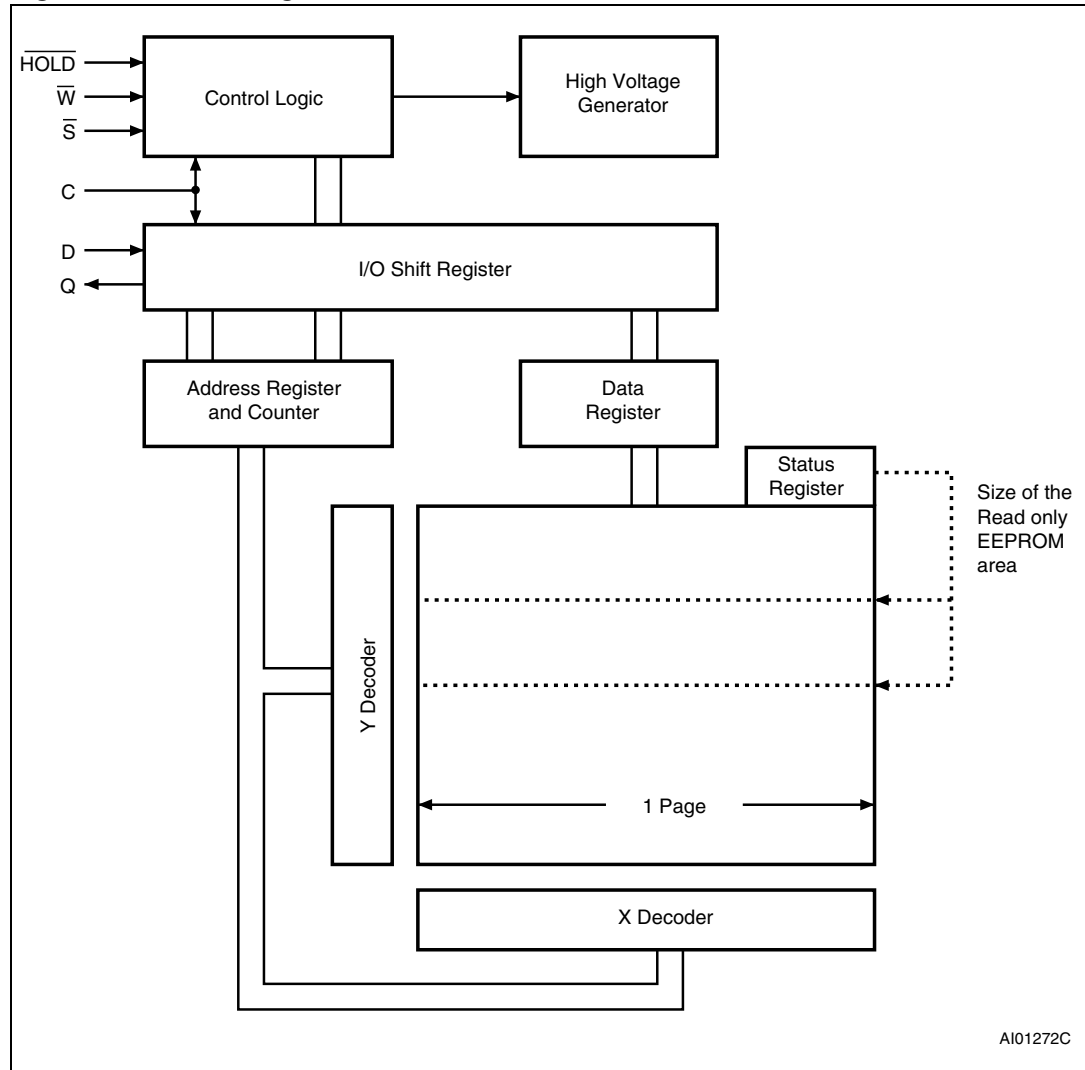
Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V _{CC}	Supply voltage	
V _{SS}	Ground	

2 Memory organization

The memory is organized as shown in [Figure 3](#).

Figure 3. Block diagram



3 Signal description

See [Figure 1: Logic diagram](#) and [Table 1: Signal names](#), for a brief overview of the signals connected to this device.

3.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

3.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

3.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

3.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

3.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

3.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3.8 Supply voltage (V_{CC})

3.8.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range must be applied (see [Table 7](#), [Table 8](#) and [Table 9](#)). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

3.8.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is defined in DC tables [12](#), [13](#), [14](#) and [15](#) as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in Standby Power mode
- deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status register values:
 - the Write Enable Latch (WEL) bit is reset to 0
 - the Write In Progress (WIP) bit is reset to 0
 - the SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. The device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [$V_{CC}(\min)$, $V_{CC}(\max)$] range defined in [Table 7](#), [Table 8](#) and [Table 9](#).

3.8.3 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC} . During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see [Figure 12](#)).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as it is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in [Table 7](#), [Table 8](#) and [Table 9](#) and the rise time must not vary faster than 1 V/ μ s.

3.8.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in [Table 7](#), [Table 8](#) and [Table 9](#)), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be any internal write cycle in progress).

4 Operating features

4.1 Hold condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) low.

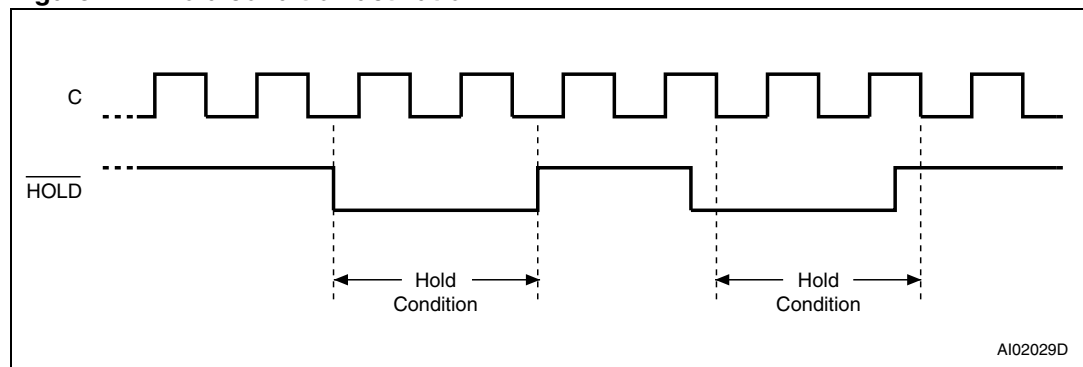
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{\text{HOLD}}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in [Figure 4](#)).

The Hold condition ends when the Hold ($\overline{\text{HOLD}}$) signal is driven high at the same time as Serial Clock (C) already being low.

[Figure 4](#) also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 4. Hold condition activation



4.2 Status Register

[Figure 3](#) shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. For a detailed description of the Status Register bits, see [Section 5.3: Read Status Register \(RDSR\)](#).

4.3 Data Protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
 - Power-up
 - Write Disable (WRDI) instruction completion
 - Write Status Register (WRSR) instruction completion
 - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{WP}$) signal is used to protect the Block Protect (BP1, BP0) bits of the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The 'last bit of the instruction' can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The 'next rising edge of Serial Clock (C)' might (or might not) be the next bus transaction for some other device on the SPI bus.

Table 2. Write-protected block size

Status Register bits		Protected block	Array addresses protected
BP1	BP0		M95128, M95128-W, M95128-R
0	0	none	none
0	1	Upper quarter	3000h - 3FFFh
1	0	Upper half	2000h - 3FFFh
1	1	Whole memory	0000h - 3FFFh

5 Instructions

Each instruction starts with a single-byte code, as summarized in [Table 3](#).
If an invalid instruction is sent (one not contained in [Table 3](#)), the device automatically deselects itself.

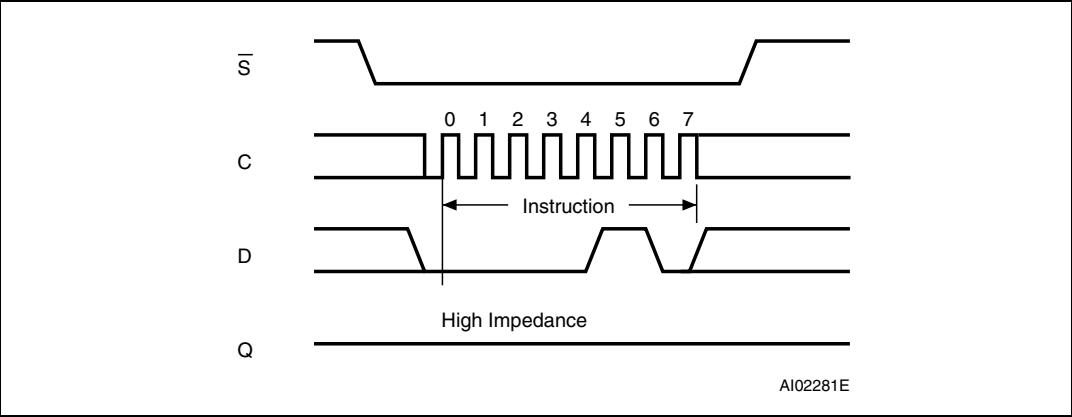
Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

5.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.
As shown in [Figure 5](#), to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 5. Write Enable (WREN) sequence



5.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

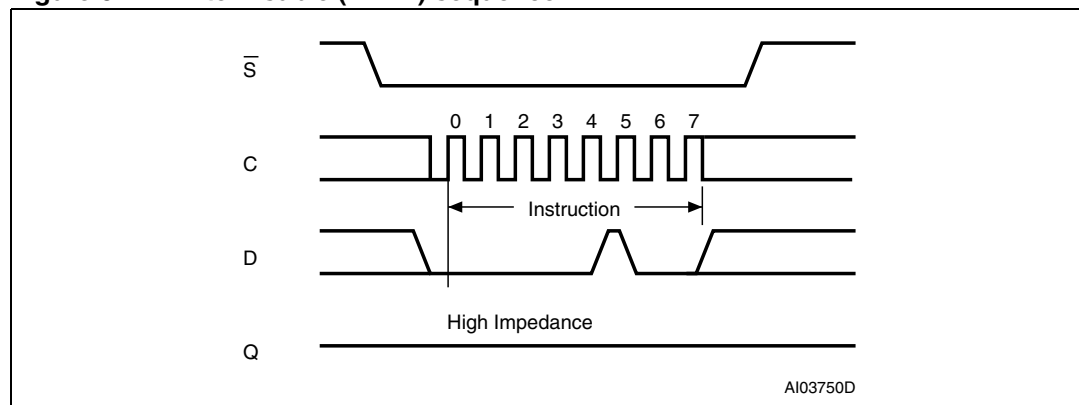
As shown in [Figure 6](#), to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 6. Write Disable (WRDI) sequence



5.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in [Figure 7](#).

The status and control bits of the Status Register are as follows:

5.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

5.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

5.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in [Table 4](#)) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

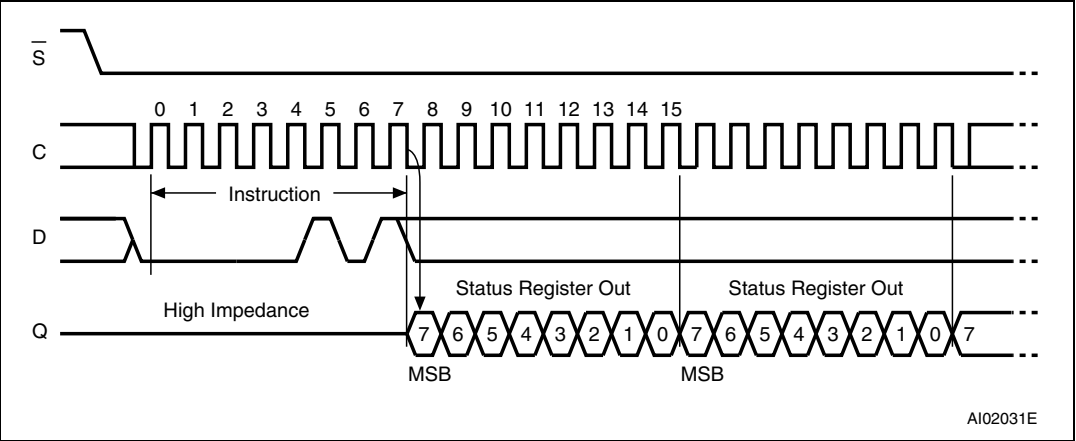
5.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 4. Status Register format

b7				b0			
SRWD	0	0	0	BP1	BP0	WEL	WIP
Status Register Write Protect				Block Protect bits		Write Enable Latch bit	Write In Progress bit

Figure 7. Read Status Register (RDSR) sequence



5.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code followed by the data byte on Serial Data input (D), and driving the Chip Select ($\overline{S}$) signal high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in [Table 16](#), [Table 17](#), [Table 19](#) and [Table 19](#)). The instruction sequence is shown in [Figure 8](#).

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W , and, 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W .

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 and SRWD bits:

- The Block protect (BP1, BP0) bits define the size of the area that is to be treated as read only, as defined in [Table 5](#).
- The SRWD bit (Status register write disable bit), in accordance with the signal read on the Write protect pin ($\overline{W}$), allows the user to set or reset the write protection mode of the Status Register itself, as shown in [Table 5](#). When in the Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1 and b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 5. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area ⁽¹⁾	Unprotected area ⁽¹⁾
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit)	Write Protected	Ready to accept Write instructions
0	0		The values in the BP1 and BP0 bits can be changed		
1	1	Hardware Protected (HPM)	Status Register is Hardware write protected	Write Protected	Ready to accept Write instructions
0	1		The values in the BP1 and BP0 bits cannot be changed		

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in [Table 5](#).

The protection features of the device are summarized in [Table 2](#).

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of whether Write Protect ($\overline{W}$) is driven high or low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven low, it is *not* possible to write to the Status Register *even* if the Write enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution.) As a consequence, all the data bytes in the memory area that are software-protected (SPM) by the Block protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

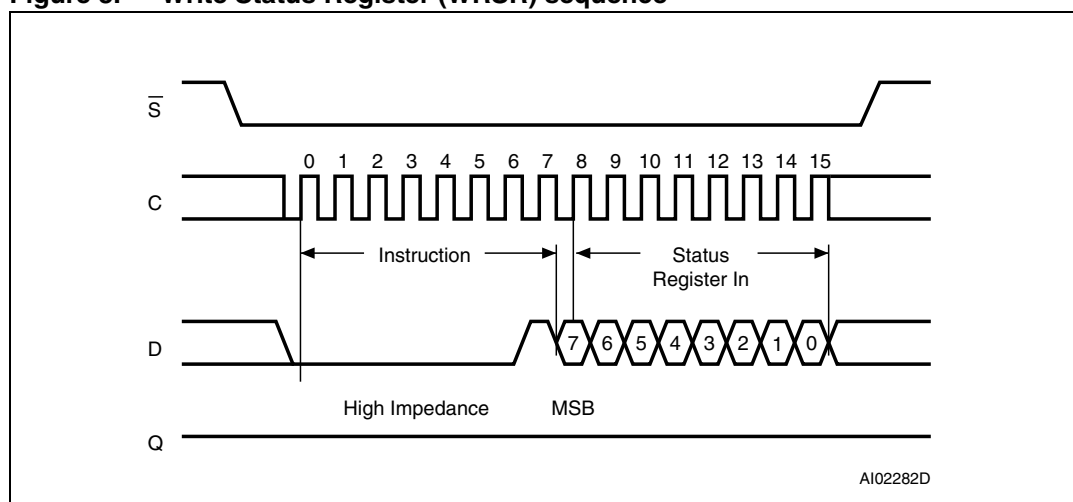
Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered:

- by setting the Status register write disable (SRWD) bit after driving Write Protect ($\overline{W}$) low
- or by driving Write Protect ($\overline{W}$) low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware-protected mode (HPM) once entered is to pull Write Protect ($\overline{W}$) high.

If Write Protect ($\overline{W}$) is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block protect (BP1, BP0) bits in the Status Register, can be used.

Figure 8. Write Status Register (WRSR) sequence



5.5 Read from Memory Array (READ)

As shown in [Figure 9](#), to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

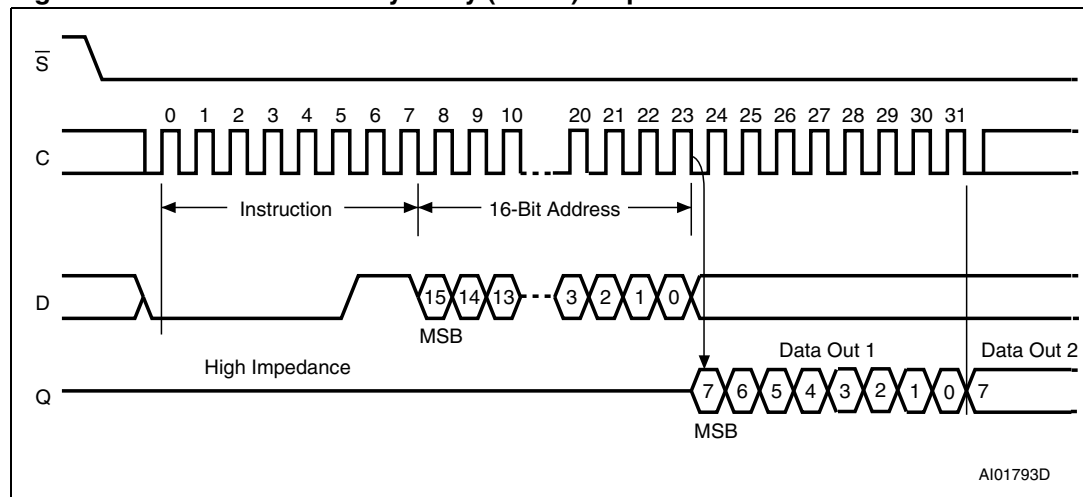
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 9. Read from Memory Array (READ) sequence



1. The most significant address bits (b15, b14) are Don't Care.

5.6 Write to Memory Array (WRITE)

As shown in [Figure 10](#), to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed write cycle, triggered by the rising edge of Chip Select ($\overline{S}$), continues for a period t_{WC} (as specified in [Table 16](#) to [Table 19](#).), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of [Figure 10](#), Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in [Figure 11](#)., the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle.

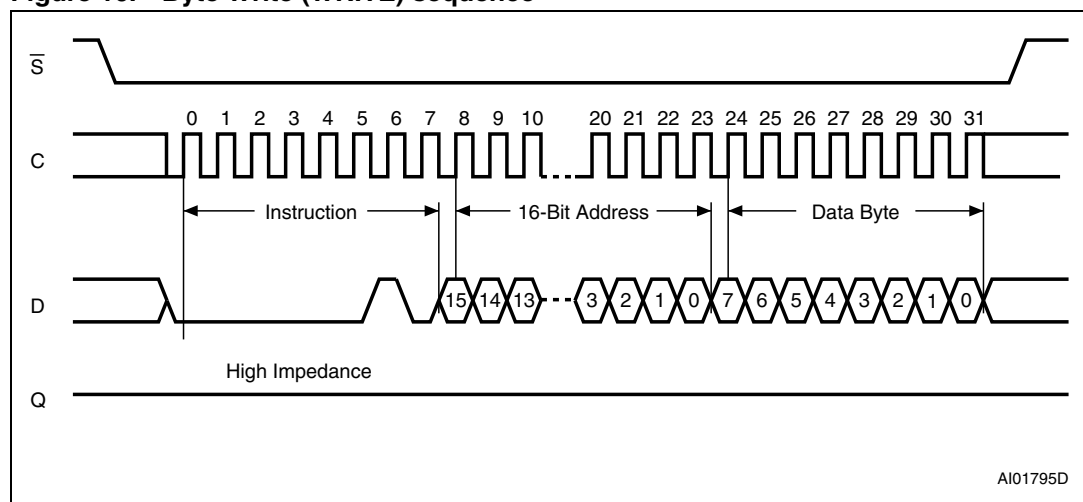
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 64 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

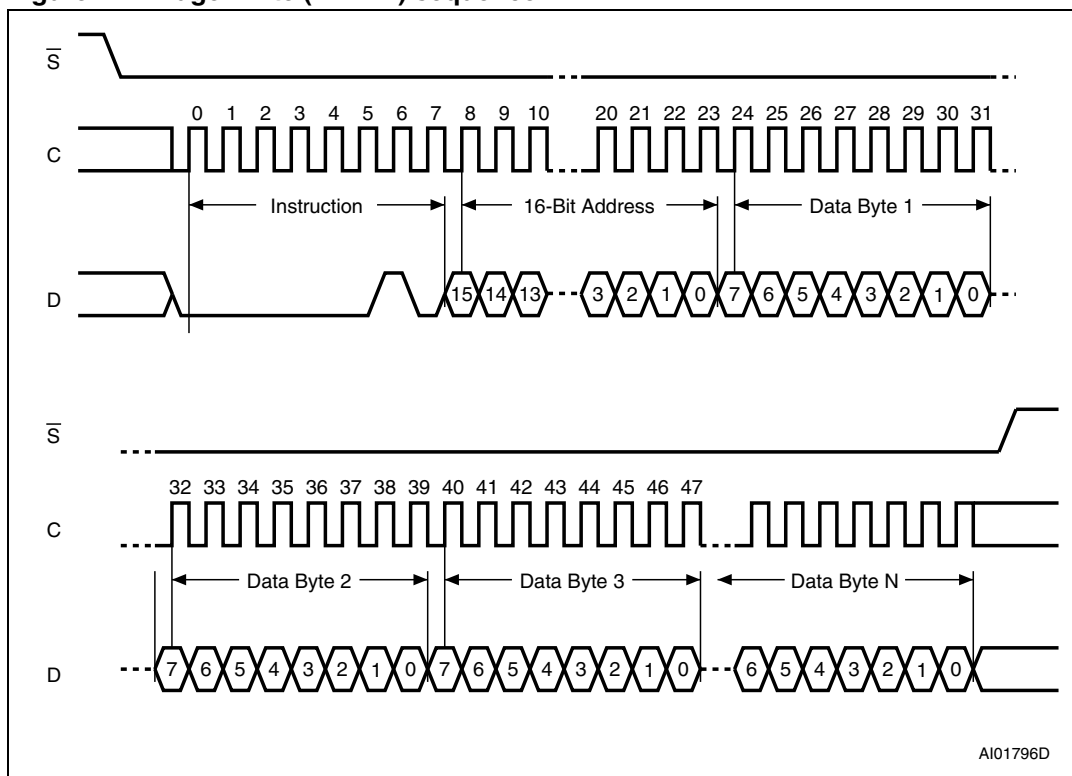
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as “0” and a programmed bit is read as “1”.

Figure 10. Byte Write (WRITE) sequence



1. The most significant address bits (b15, b14) are Don't Care.

Figure 11. Page Write (WRITE) sequence

1. The most significant address bits (b15, b14) are Don't Care.

5.6.1 ECC (error correction code) and write cycling

Most M95128, M95128-W and M95128-R devices offer an ECC (error correction code) logic which compares each 4-byte word with 6 EEPROM bits of ECC (the list of concerned devices is defined in [Table 24: Available M95128x products \(package, voltage range, temperature grade\)](#)). As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by packets of 4 bytes in order to benefit from the larger amount of write cycles.

The maximum number of write cycles is qualified at 1 Million (1 000 000) write cycles, using a cycling routine that writes to the device by multiples of 4-byte packets.

6 Delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

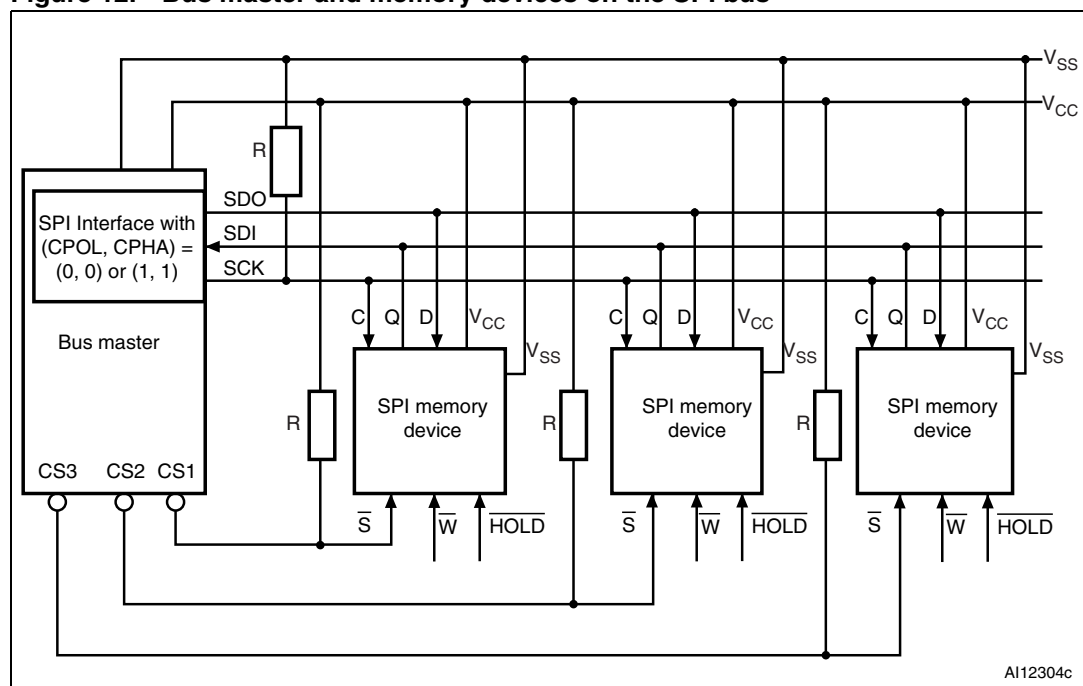
7 Connecting to the SPI bus

These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 12. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 12 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data Output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 12*) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master might enter a state where all inputs/outputs SPI bus would be in high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\bar{S}$ line is pulled high): this will ensure that $\bar{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 k Ω

7.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

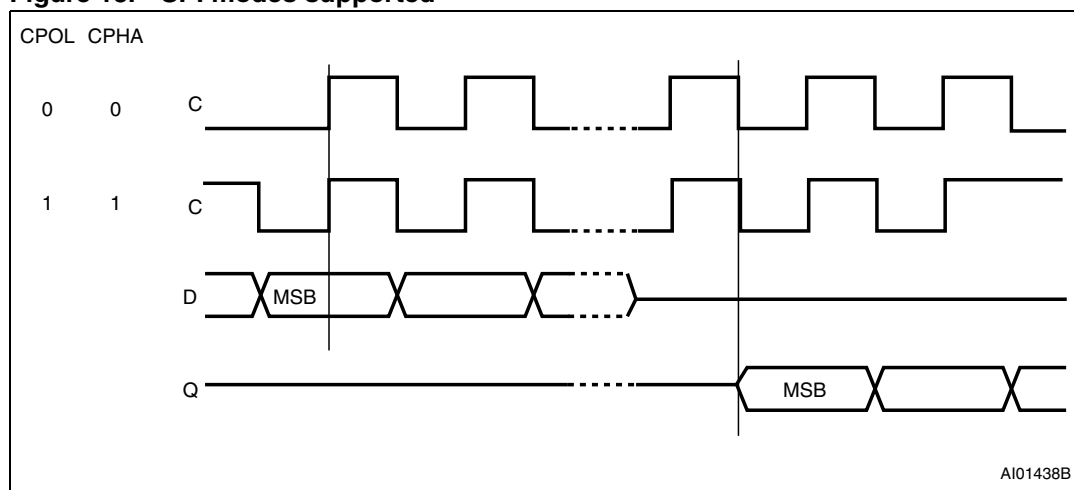
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in [Figure 13](#), is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 13. SPI modes supported



8 Maximum rating

Stressing the device outside the ratings listed in [Table 6](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
T_{LEAD}	Lead temperature during soldering	See note ⁽¹⁾		°C
V_O	Output voltage	-0.50	$V_{CC}+0.6$	V
V_I	Input voltage	-0.50	6.5	V
I_{OL}	DC output current ($Q = 0$)		5	mA
I_{OH}	DC output current ($Q = 1$)		-5	mA
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model) ⁽²⁾	-4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU

2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 p F, R1 = 1500 Ω, R2 = 500 Ω).

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating conditions (M95128)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 3)	−40	125	°C

Table 8. Operating conditions (M95128-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	−40	85	°C
	Ambient operating temperature (device grade 3)	−40	125	°C

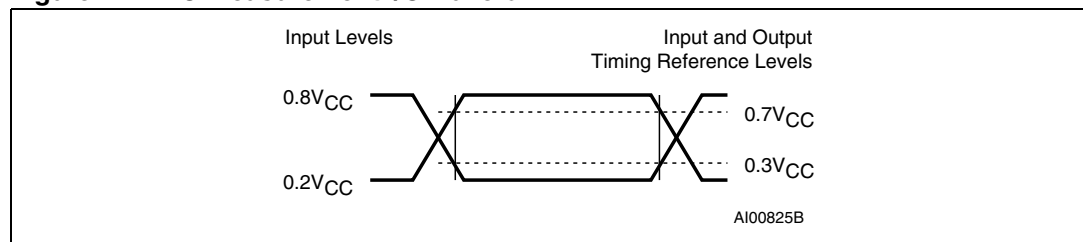
Table 9. Operating conditions (M95128-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	−40	85	°C

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input pulse voltages	0.2V _{CC} to 0.8V _{CC}		V
	Input and output ⁽¹⁾ timing reference voltages	0.3V _{CC} to 0.7V _{CC}		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC measurement I/O waveform**Table 11. Capacitance⁽¹⁾**

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	$V_{OUT} = 0\text{ V}$		8	pF
C_{IN}	Input capacitance (D)	$V_{IN} = 0\text{ V}$		8	pF
	Input capacitance (other pins)	$V_{IN} = 0\text{ V}$		6	pF

1. Sampled only, not 100% tested, at $T_A = 25\text{ °C}$ and a frequency of 5 MHz.

Table 12. DC characteristics (M95128, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{LO}	Output leakage current	$\bar{S} = V_{CC}, V_{OUT} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{CC}	Supply current	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 5 \text{ V}, Q = \text{open}$		4	mA
		$C = 0.1V_{CC}/0.9V_{CC}$ at 10 MHz, $V_{CC} = 5 \text{ V}, Q = \text{open}$		8	mA
I_{CC1}	Supply current (Standby Power mode)	$\bar{S} = V_{CC}, V_{CC} = 5 \text{ V},$ $V_{IN} = V_{SS} \text{ or } V_{CC}$		5	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
$V_{OL}^{(1)}$	Output low voltage	$I_{OL} = 2 \text{ mA}, V_{CC} = 5 \text{ V}$		0.4	V
$V_{OH}^{(1)}$	Output high voltage	$I_{OH} = -2 \text{ mA}, V_{CC} = 5 \text{ V}$	$0.8 V_{CC}$		V
$V_{RES}^{(2)}$	Internal reset threshold voltage		2.5	4.0	V

1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not 100% tested.

Table 13. DC characteristics (M95128-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{LO}	Output leakage current	$\bar{S} = V_{CC}, V_{OUT} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{CC}	Supply current (Read)	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 2.5 \text{ V}, Q = \text{open}$		3	mA
		$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 5 \text{ V}, Q = \text{open}$		5	mA
$I_{CC0}^{(1)}$	Supply current (Write)	During $t_{W}, \bar{S} = V_{CC}, 2.5 \text{ V} < V_{CC} < 5.5 \text{ V}$		5	mA
I_{CC1}	Supply current (Standby Power mode)	$\bar{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC},$ $2.5 \text{ V} < V_{CC} < 5.5 \text{ V}$		5	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$V_{CC} = 2.5 \text{ V}$ and $I_{OL} = 1.5 \text{ mA}$ or $V_{CC} = 5 \text{ V}$ and $I_{OL} = 2 \text{ mA}$		0.4	V
V_{OH}	Output high voltage	$V_{CC} = 2.5 \text{ V}$ and $I_{OH} = -0.4 \text{ mA}$ or V_{CC} $= 5 \text{ V}$ and $I_{OH} = -2 \text{ mA}$	$0.8 V_{CC}$		V
$V_{RES}^{(2)}$	Internal reset threshold voltage		1.0	1.65	V

1. Characterized value, not tested in production.
2. Characterized only, not 100% tested.

Table 14. DC characteristics (M95128-W, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}, V_{OUT} = V_{SS} \text{ or } V_{CC}$		± 2	μA
I_{CC}	Supply current (Read)	$C = 0.1V_{CC}/0.9V_{CC}$ at 5 MHz, $V_{CC} = 2.5 \text{ V}$, Q = open		3	mA
$I_{CC0}^{(1)}$	Supply current (Write)	During t_W , $\overline{S} = V_{CC}$, $2.5 \text{ V} < V_{CC} < 5.5 \text{ V}$		6	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}, V_{IN} = V_{SS} \text{ or } V_{CC}$ $2.5 \text{ V} < V_{CC} < 5.5 \text{ V}$,		5	μA
V_{IL}	Input low voltage		-0.45	$0.3 V_{CC}$	V
V_{IH}	Input high voltage		$0.7 V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$V_{CC} = 2.5 \text{ V}$ and $I_{OL} = 1.5 \text{ mA}$ or $V_{CC} = 5 \text{ V}$ and $I_{OL} = 2 \text{ mA}$		0.4	V
V_{OH}	Output high voltage	$V_{CC} = 2.5 \text{ V}$ and $I_{OH} = -0.4 \text{ mA}$ or $V_{CC} = 5 \text{ V}$ and $I_{OH} = -2 \text{ mA}$	$0.8 V_{CC}$		V
$V_{RES}^{(2)}$	Internal reset threshold voltage		1.0	1.65	V

1. Characterized value, not tested in production.

2. Characterized only, not 100% tested.

Table 15. DC characteristics (M95128-R)

Symbol	Parameter	Test condition ⁽¹⁾	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	μA
I_{LO}	Output leakage current	$S = V_{CC}$, voltage applied on $Q = V_{SS}$ or V_{CC}		± 2	μA
I_{CCR}	Supply current (Read)	$V_{CC} = 1.8 V$, $C = 0.1 V_{CC}$ or $0.9V_{CC}$, $f_C = 2 MHz$, $Q = open$		1	mA
		$V_{CC} = 2.5 V$, $C = 0.1 V_{CC}$ or $0.9V_{CC}$, $f_C = 2 MHz$, $Q = open$		3	mA
I_{CC1}	Supply current (Standby)	$V_{CC} = 5.0 V$, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		5	μA
		$V_{CC} = 2.5 V$, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		3	μA
		$V_{CC} = 1.8 V$, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		3	μA
V_{IL}	Input low voltage	$2.5V < V_{CC} < 5.5V$	-0.45	$0.3V_{CC}$	V
		$1.8V < V_{CC} < 2.5V$	-0.45	$0.25V_{CC}$	V
V_{IH}	Input high voltage	$2.5V < V_{CC} < 5.5V$	$0.7V_{CC}$	$V_{CC}+1$	V
		$1.8V < V_{CC} < 2.5V$	$0.75V_{CC}$	$V_{CC}+1$	V
V_{OL}	Output low voltage	$V_{CC} = 2.5 V$, $I_{OL} = 1.5 mA$ or $V_{CC} = 5.5 V$, $I_{OL} = 2 mA$		$0.2V_{CC}$	V
		$V_{CC} = 1.8 V$, $I_{OL} = 0.15 mA$		0.3	V
V_{OH}	Output high voltage	$V_{CC} = 2.5 V$, $I_{OH} = -0.4 mA$, or $V_{CC} = 5.5 V$, $I_{OH} = -2 mA$, or $V_{CC} = 1.8 V$, $I_{OH} = -0.1 mA$	$0.8V_{CC}$		V
$V_{RES}^{(2)}$	Internal reset threshold voltage		1.0	1.65	V

1. If the application uses the M95128-R device with $2.5 V < V_{CC} < 5.5 V$ and $-40^\circ C < T_A < +85^\circ C$, please refer to [Table 17: AC characteristics \(M95128-W, device grade 6\)](#) instead of the above table.

2. Characterized only, not 100% tested.

Table 16. AC characteristics (M95128, device grade 3)

Test conditions specified in Table 10 and Table 7					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	45		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	45		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		2	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		2	μs
t_{DVCH}	t_{DSU}	Data in setup time	10		ns
t_{CHDX}	t_{DH}	Data in hold time	10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		40	ns
t_{CLQV}	t_V	Clock low to output valid		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		40	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output high-Z		40	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(\max)$

2. Value guaranteed by characterization, not 100% tested in production.

Table 17. AC characteristics (M95128-W, device grade 6)

Test conditions specified in Table 10 and Table 8					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	90		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	90		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		50	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(\max)$

2. Value guaranteed by characterization, not 100% tested in production.

Table 18. AC characteristics (M95128-W, device grade 3)

Test conditions specified in Table 10 and Table 8					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
$t_{CH}^{(1)}$	t_{CLH}	Clock high time	90		ns
$t_{CL}^{(1)}$	t_{CLL}	Clock low time	90		ns
$t_{CLCH}^{(2)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(2)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(2)}$	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(2)}$	t_{RO}	Output rise time		50	ns
$t_{QHQL}^{(2)}$	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
$t_{HLQZ}^{(2)}$	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(\max)$

2. Value guaranteed by characterization, not 100% tested in production.

Table 19. AC characteristics (M95128-R)

Test conditions specified in Table 10 and Table 9 ⁽¹⁾					
Symbol	Alt.	Parameter	Min. ⁽²⁾	Max. ⁽²⁾	Unit
f_C	f_{SCK}	Clock frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	200		ns
t_{CHSL}		$\overline{S}$ not active hold time	200		ns
$t_{CH}^{(3)}$	t_{CLH}	Clock high time	200		ns
$t_{CL}^{(3)}$	t_{CLL}	Clock low time	200		ns
$t_{CLCH}^{(4)}$	t_{RC}	Clock rise time		1	μs
$t_{CHCL}^{(4)}$	t_{FC}	Clock fall time		1	μs
t_{DVCH}	t_{DSU}	Data in setup time	40		ns
t_{CHDX}	t_{DH}	Data in hold time	50		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	140		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	90		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
$t_{SHQZ}^{(4)}$	t_{DIS}	Output disable time		250	ns
t_{CLQV}	t_V	Clock low to output valid		150	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
$t_{QLQH}^{(4)}$	t_{RO}	Output rise time		100	ns
$t_{QHQL}^{(4)}$	t_{FO}	Output fall time		100	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		100	ns
$t_{HLQZ}^{(4)}$	t_{HZ}	$\overline{HOLD}$ low to output high-Z		250	ns
t_W	t_{WC}	Write time		5	ms

1. If the application uses the M95128-R at $2.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ and $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, please refer to [Table 17](#) instead of the above table.
2. This is preliminary data.
3. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(\text{max})$
4. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial input timing

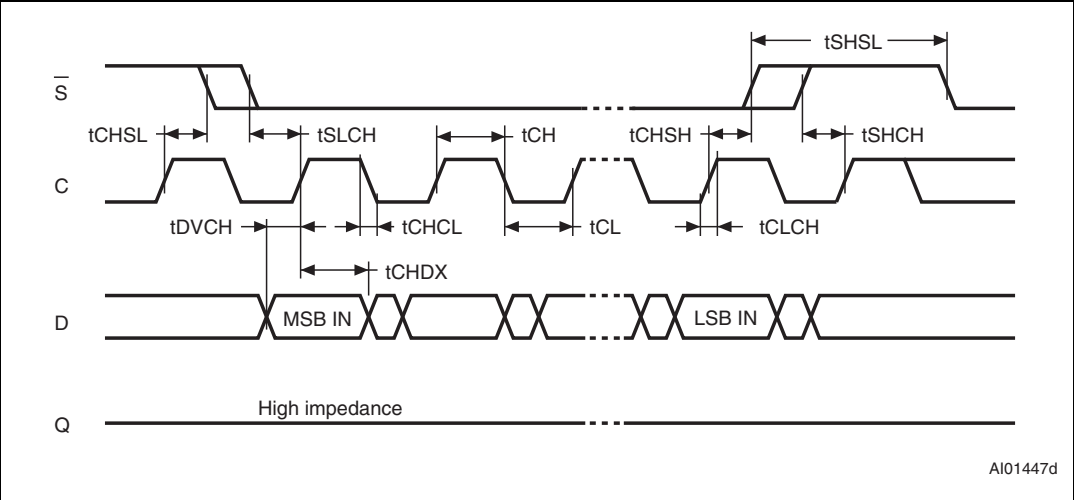


Figure 16. Hold timing

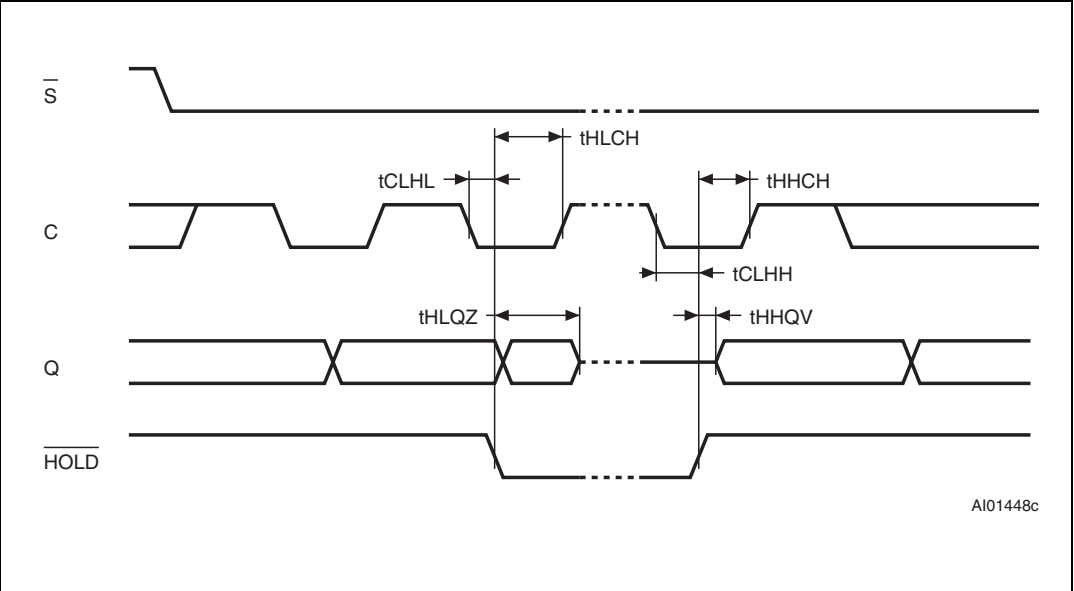
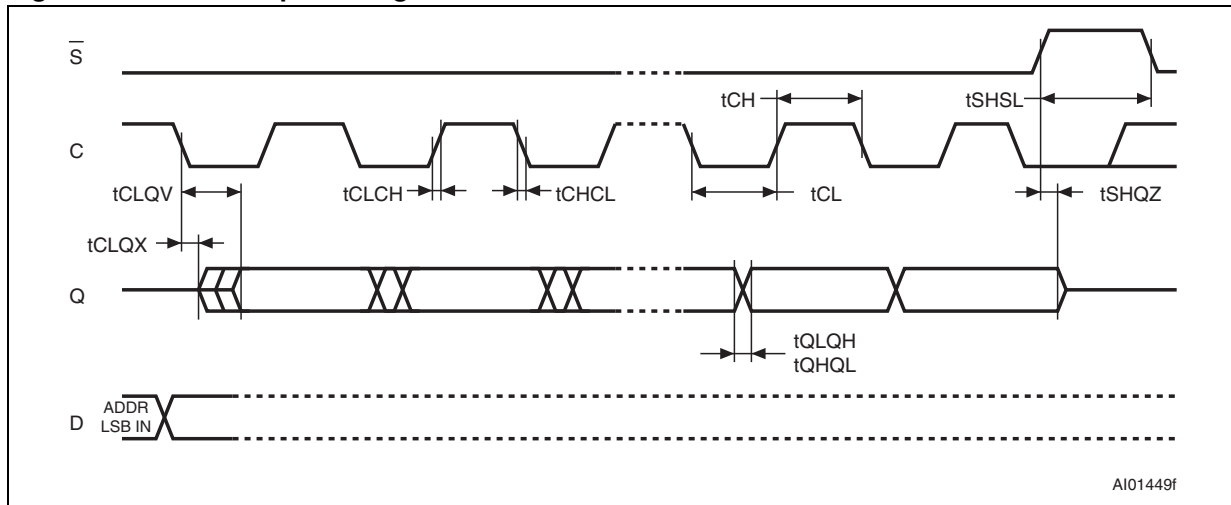


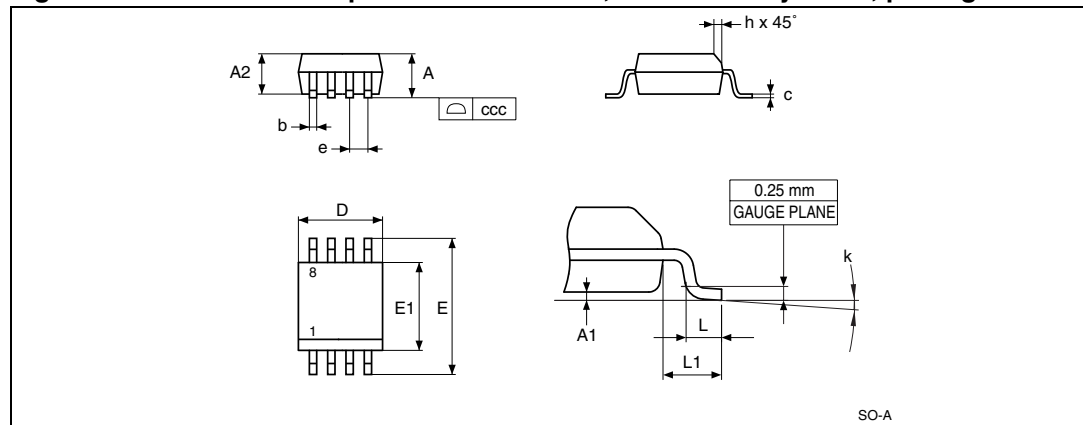
Figure 17. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 18. SO8N – 8-lead plastic small outline, 150 mils body width, package outline

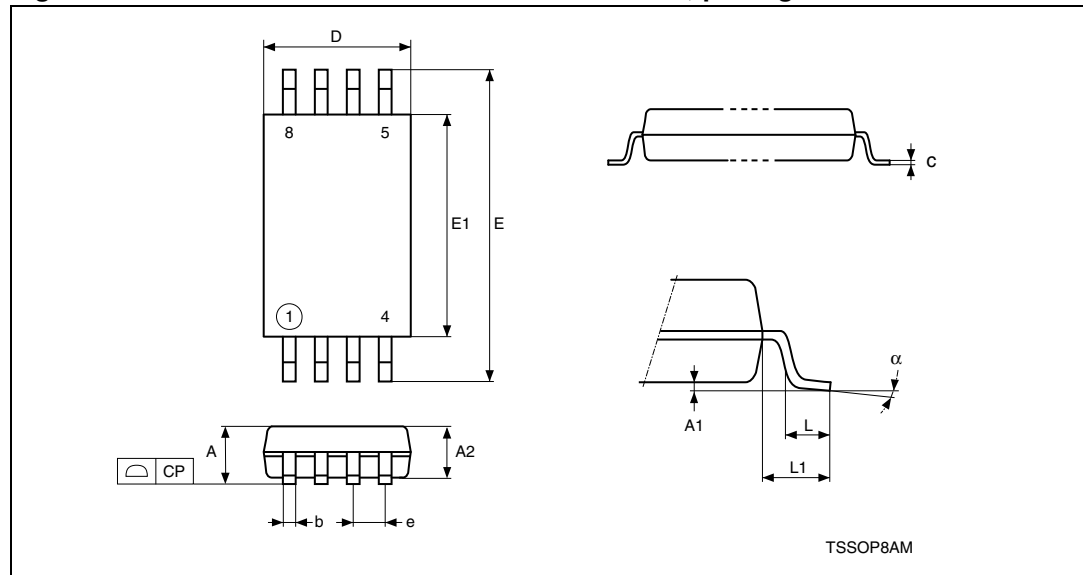


1. Drawing is not to scale.

Table 20. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.10	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.10			0.0039
D	4.90	4.80	5.00	0.1929	0.189	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	–	–	0.05	–	–
h		0.25	0.50		0.0098	0.0197
k		0°	8°		0°	8°
L		0.40	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

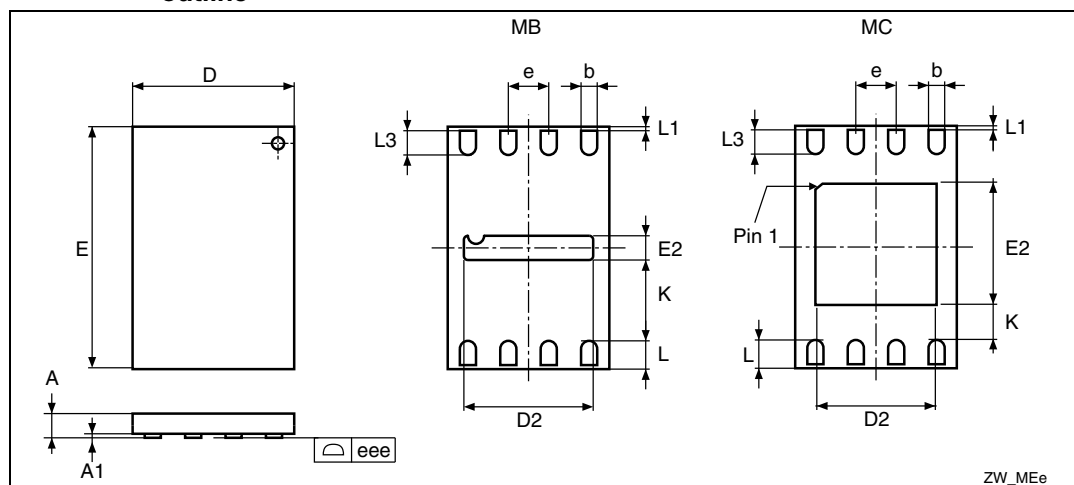
Figure 19. TSSOP8 – 8-lead thin shrink small outline, package outline

1. Drawing is not to scale.

Table 21. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	—	—	0.0256	—	—
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N (number of leads)	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 20. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline

1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS} . It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 22. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches ⁽¹⁾		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MB)		0.800			0.0315	
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee ⁽²⁾		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

11 Part numbering

Table 23. Ordering information scheme

Example:	M95128	–	W	MN	6	T	P	/P
Device type								
M95 = SPI serial access EEPROM								
Device function								
128 = 128 Kbit (16384 x 8)								
Operating voltage								
blank = $V_{CC} = 4.5$ to 5.5 V								
W = $V_{CC} = 2.5$ to 5.5 V								
R = $V_{CC} = 1.8$ to 5.5 V								
Package								
MN = SO8 (150 mils width)								
DW = TSSOP8 (169 mils width)								
MB or MC = UDFPN8 (MLP8 2 x 3 mm)								
Device grade								
6 = Industrial temperature range, -40 to 85 °C.								
Device tested with standard test flow								
3 = Device tested with high reliability certified flow ⁽¹⁾								
Automotive temperature range (-40 to 125 °C)								
Option								
blank = Standard packing								
T = Tape and reel packing								
Plating technology								
P or G = ECOPACK2 [®] (RoHs compliant and Halogen-free)								
Process⁽²⁾								
/P or /PC = DP26% Chartered								

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a co.
2. The Process letter /P applies only to Grade 3 devices.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 24. Available M95128x products (package, voltage range, temperature grade)

Package	M95128-R (1.8 V to 5.5 V)	M95128-W (2.5 V to 5.5 V)	M95128 (4.5 V to 5.5 V)
SO8N (MN)	Grade 6	Grade 6 Grade 3 ⁽¹⁾	Grade 3 ⁽¹⁾
UFDFPN8 (MLP8) 2 × 3 mm (MB)	Grade 6	-	-
TSSOP (DW)	Grade 6	Grade 3 ⁽¹⁾	-

1. Grade 3 products (without ECC) are codified as /P and /PC in [Table 23: Ordering information scheme](#).

12 Revision history

Table 25. Document revision history

Date	Revision	Changes
17-Nov-1999	2.1	New -V voltage range added (including the tables for DC characteristics, AC characteristics, and ordering information).
07-Feb-2000	2.2	New -V voltage range extended to M95256 (including AC characteristics, and ordering information).
22-Feb-2000	2.3	tCLCH and tCHCL, for the M95xxx-V, changed from 1μs to 100ns
15-Mar-2000	2.4	-V voltage range changed to 2.7-3.6V
29-Jan-2001	2.5	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Illustrations and Package Mechanical data updated
12-Jun-2001	2.6	Correction to header of Table 12B TSSOP14 Illustrations and Package Mechanical data updated Document promoted from Preliminary Data to Full Data Sheet
08-Feb-2002	2.7	Announcement made of planned upgrade to 10 MHz clock for the 5V, -40 to 85°C, range.
09-Aug-2002	2.8	M95128 split off to its own datasheet. Data added for new and forthcoming products, including availability of the SO8 narrow package.
24-Feb-2003	2.9	Omission of SO8 narrow package mechanical data remedied
26-Jun-2003	2.10	-V voltage range removed
21-Nov-2003	3.0	Table of contents, and Pb-free options added. -S voltage range extended to -R. $V_{IL}(\text{min})$ improved to -0.45V
17-Mar-2004	4.0	Absolute Maximum Ratings for $V_{IO}(\text{min})$ and $V_{CC}(\text{min})$ changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified
21-Oct-2004	5.0	M95128 datasheet merged back in. Product List summary table added. AEC-Q100-002 compliance. Device Grade information clarified. tHHQX corrected to tHHQV. 10MHz product becomes standard

Table 25. Document revision history (continued)

Date	Revision	Changes
13-Apr-2006	6	New M95128 datasheet extracted from the M95128/256 datasheet. Order of sections modified. <i>ECC (error correction code) and Write cycling</i> paragraph added. <i>Section 3.8: Supply voltage (VCC)</i> added and information removed below <i>Section 4: Operating features</i>. Power up state removed below <i>Section 6: Delivery state</i>. <i>Figure 13: SPI modes supported</i> modified and <i>Note 2</i> added. I_{CC1} specified over the whole V_{CC} range and I_{CC0} added to <i>Table 13</i>, <i>Table 14</i> and <i>Table 15</i>. I_{CC} specified over the whole V_{CC} range in <i>Table 13</i>. t_{CHHL} and t_{CHHH} replaced by t_{CLHL} and t_{CLHH}, respectively. <i>Figure 16: Hold timing</i> modified. <i>Process</i> letter and <i>Note 1</i> added to <i>Table 23: Ordering information scheme</i>. "<i>AC Characteristics (M95128, Device Grade 6)</i>" Table (for 10MHz frequency) removed. <i>Note 1</i> removed from <i>Table 19: AC characteristics (M95128-R)</i>. T_A added to <i>Table 6: Absolute maximum ratings</i>. PDIP8 (BN) and SO8 wide (MW) packages removed. M95128-W and M95128-R are no longer under development. Test conditions changed for V_{OL} and V_{OH} in <i>Section Table 14.: DC characteristics (M95128-W, device grade 3)</i>.
27-Jun-2006	7	<i>Figure 12: Bus master and memory devices on the SPI bus</i> modified. SO8N package specifications updated (see <i>Table 20</i> and <i>Figure 18</i>). V Process specified and A Process replaced by P in <i>Table 23: Ordering information scheme</i>.
04-Oct-2007	8	<i>Section 3.8: Supply voltage (VCC)</i>, <i>Section 4.3: Data Protection and protocol control</i>, <i>Section 5.4: Write Status Register (WRSR)</i>, <i>Section 5.6: Write to Memory Array (WRITE)</i> and <i>Section 5.6.1: ECC (error correction code) and Write cycling</i> updated. <i>Note</i> removed below <i>Figure 12: Bus master and memory devices on the SPI bus</i>, replaced by paragraph. Test conditions modified for I_{CC1} and I_{CC0} in <i>Table 15: DC characteristics (M95128-R)</i>. AC characteristics values added for f_C frequency = 10 MHz in <i>Table 16: AC characteristics (M95128, device grade 3)</i>. t_W modified in <i>Table 19: AC characteristics (M95128-R)</i>. <i>Section 10: Package mechanical data</i>: – UDFFPN8 package added – Package mechanical inch values calculated from mm and rounded to 4 decimal digits <i>Table 24: Available M95128x products (package, voltage range, temperature grade)</i> added. Blank removed below Plating technology, first note removed, process A added and process V removed in <i>Table 23: Ordering information scheme</i>.
15-Jan-2008	9	<i>Section 3.7: VSS ground</i> added. <i>Section 3.8.2: Device reset</i>, <i>Section 3.8.4: Power-down</i> and <i>Section 5.6.1: ECC (error correction code) and Write cycling</i> modified. V_{IL} and V_{IH} modified in <i>Table 15: DC characteristics (M95128-R)</i>. <i>Table 24: Available M95128x products (package, voltage range, temperature grade)</i> updated.

Table 25. Document revision history (continued)

Date	Revision	Changes
11-Jul-2008	10	M95128, device grade 3 devices is now offered at 10 MHz frequency. <i>Section 3.8: Supply voltage (VCC) on page 10</i> and <i>Section 5.4: Write Status Register (WRSR) on page 18</i> updated. <i>Table 15: DC characteristics (M95128-R) on page 30</i> modified. t_{CH} and t_{CL} modified in <i>Table 16: AC characteristics (M95128, device grade 3) on page 31</i> . <i>Figure 15: Serial input timing, Figure 16: Hold timing and Figure 17: Serial output timing</i> modified. Process A removed from <i>Table 23: Ordering information scheme</i> . Small text changes.
17-Feb-2009	11	<i>Section 3.8: Supply voltage (VCC)</i> and <i>Section 5.4: Write Status Register (WRSR)</i> updated. Note added to <i>Section 5.6: Write to Memory Array (WRITE)</i> . I_{CC} modified in <i>Table 12: DC characteristics (M95128, device grade 3)</i> . V_{RES} added to DC characteristics tables <i>12, 13, 14</i> and <i>15</i> . Note added to <i>Table 19: AC characteristics (M95128-R)</i> . Note added below <i>Figure : .</i> Small text changes.
12-Jan-2010	12	<i>Section 5.6.1: ECC (error correction code) and write cycling</i> modified (applies to all devices). T_{LEAD} , I_{OL} and I_{OH} added to <i>Table 6: Absolute maximum ratings</i> . Note added to <i>Table 15: DC characteristics (M95128-R)</i> . <i>Process</i> modified in <i>Table 23: Ordering information scheme</i> . All packages are ECOPACK2 compliant.
02-Mar-2010	13	<i>Section 5.6.1: ECC (error correction code) and write cycling</i> and <i>Table 24: Available M95128x products (package, voltage range, temperature grade)</i> updated.
04-Jan-2012	14	Updated UDFPN8 package data.

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