



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM/11/6300
Notification Date 03/08/2011

**Capacity extension in the ST site of Longgang, China
and ECOPACK 2 conversion completion for the TO-220FP package**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	18-Apr-2011
Forecasted availability date of samples for customer	25-Apr-2011
Forecasted date for STMicroelectronics change Qualification Plan results availability	01-Mar-2011
Estimated date of changed product first shipment	07-Jun-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Multiple types of changes
Reason for change	Capacity expansion and ECOPACK 2 program conversion
Description of the change	Progressing in the plan for rationalizing the manufacturing processes and progressively expand production capacity, please be informed that the products housed in the TO-220FP package, currently manufactured in the Shenzhen (China) plant, will be from now either available from the site of Longgang (China). At the same time, to meet the so called "Halogen-Free" requirements of the market, ASD&IPAD Division is also completing the conversion of its TO-220FP to the ECOPACKfi2 grade. For the complete list of the part numbers affected by this change, please refer to the attached Products list.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Internal codification, product marking and labeling, Q.A. number
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Giuffrida, Antonino	Division Marketing Manager
Caizzone, Francesco	Division Product Manager
Vitali, Gian Luigi	Division Q.A. Manager

WHAT:

Progressing in the plan for **rationalizing the manufacturing processes** and progressively expand **production capacity**, please be informed that the products housed in the TO-220FP package, currently manufactured in the Shenzhen (China) plant, will be from now either available from the site of **Longgang** (China).

At the same time, to meet the so called "Halogen-Free" requirements of the market, ASD&IPAD Division is also completing the conversion of its **TO-220FP** to the **ECOPACK®2** grade.

For the complete list of the **part numbers** affected by this change, please refer to the attached Products list.

WHY:

This expansion will increase our **ECOPACK®2 manufacturing global capacity** for a better **service** to our Customers on the affected products, optimizing ST's **leading-edge** Longgang packaging and testing facility in China.

HOW:

This capacity expansion will be achieved by keeping **same processes** currently used in the Shenzhen site, maintaining unaltered the **electrical, dimensional** and **thermal** parameters and keeping unchanged all informations reported in the relevant product datasheets. There is no variation in the **packing process** as well and in the **standard delivery quantities** either.

All verifications are included in the qualification program.

The products will be delivered **ECOPACK®2** from the very beginning from the Longgang site, meaning in compliance with ST's ECOPACK®2 grade defined as follows:

1. **RoHS*** compliant, including with exemptions.
2. 500ppm maximum of **Antimony** as oxide or organic compound in each organic assembly material (glue, substrate, mold compound, housing...).
3. 900ppm maximum of [**Bromine + Chlorine**] in each organic assembly material with **Bromine** limited to 450 ppm.

() Restriction of the use of certain Hazardous Substances according to European Directive 2002/95/CE.*

The conversion to **ECOPACK®2 grade** will also be fully implemented in the current manufacturing site in **Shenzhen**.

Qualification program and results:

The **qualification program** consists of comparative **electrical characterizations, construction analysis** and **reliability tests**. The related qualification plans are attached to the present document.

WHEN:

The **mass production** from the Longgang site is planned for the end of **Q2-2011**. **Samples of test vehicles** are available from now except for AC Switches from the Longgang site that will be available by wk 21-2011.

Other samples of devices produced in the Longgang plant will be available **on request** with lead time depending on the qualification schedule of each product family.

Production start and **first shipments** will occur as indicated in the table below:

Product Family	Production Start (from wk...)		1st Shipments (from wk...)	
	ECOPACK®2 in Shenzhen site	Manufacturing in Longgang site	ECOPACK®2 in Shenzhen site	Manufacturing in Longgang site
Power MOSFET	Now	wk 16-2011	Now	wk 20-2011
Power Bipolar	Now	wk 16-2011	Now	wk 20-2011
IGBTs	Now	wk 16-2011	Now	wk 20-2011
IPC	wk 16-2011	wk 16-2011	wk 20-2011	wk 20-2011
Power Rectifiers	wk 16-2011	wk 16-2011	wk 20-2011	wk 20-2011
AC switches	wk 16-2011	wk 28-2011	wk 20-2011	wk 34-2011

Absence of acknowledgement of this PCN within **30 days** of receipt will constitute acceptance of the change. After an acknowledgement, unless otherwise previously agreed to in writing for a specific process change requirement or for device specific requirements, absence of additional response within **90 days** of receipt of this PCN will constitute acceptance of the change. Shipments may in any case start earlier with the customer's **written agreement**.

Marking and traceability:

Unless otherwise stated by customer specific requirement, parts assembled in the Longgang plant will be **differentiated** as indicated as below:

Assembly location	Assy plant	Seq. nbr	Diffusion plant	Country of origin	Date Code (3 digits)
Longgang (New)	G4	LLL	XX	CHN	YWW Y = 1 digit indicating the year WW = 2 digits indicating the week number
Shenzhen (current)	GK	LLL	XX	CHN	

The **marking** for the components **ECOPACK®2** graded will be differentiated with an **additional letter "G"** that will be printed to the **right of the "ST" logo**, as shown below:



The full **traceability** of the parts assembled in the Longgang plant will be ensured by the **date code**, by an **internal codification**, and by the **Q.A. number**.

Annex:

- Related **Qualification Plans** or **Reliability Reports**.



Reliability Report On TO-220FP ECOPACK®2 Capacity extension - Longgang (China)

General Information		Locations	
Product Lines	BT07-EZ62-EZ5L	Wafer fab	Ang Mo Kio (Singapore)
Product Description	N-Channel Power MOSFET NPN Power BIPOLAR	Assembly plant	Longgang (China)
Commercial Products	BUL1203EP STP4NK60ZFP STF20NK50Z	Reliability Lab	IMS-APM Catania Reliability Lab
Product Group	IMS – APM		
Product division	Power Transistor Division		
Package	TO-220FP		
Silicon Process technology	N-Channel Power MOSFET NPN Power BIPOLAR		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	February-2011	10	G.De Luca	G.Falcone	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.



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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Assembly and Testing qualification of TO-220FP package of Longgang (China).

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



4 DEVICE CHARACTERISTICS

4.1 Device description

Power Bipolar, Power MOSFET technology.

4.2 Construction note

D.U.T.: BUL1203EP LINE: BT07 PACKAGE: TO-220FP

Wafer/Die fab. Information	
Wafer fab manufacturing location	AMK (Singapore)
Technology	Planar NPN Power BIPOLAR
Die finishing back side	Ti/Ni/Au
Die size	3490 x 3390 μm^2
Metal	Al
Passivation type	P-Vapox

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Longgang (China)
Package description	TO-220FP
Molding compound	Epoxy Resin
Frame material	Raw Copper - Selected Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Base – 7 mils Al Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Longgang (China)
Tester	IP TEST



D.U.T.: STP4NK60ZFP LINE: EZ62 PACKAGE: TO-220FP

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK 6"
Technology	Power MOSFET SuperMesh™ Technology
Die finishing back side	Ti/Ni/Au
Die size	3190 x 2660 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK 6"
Test program	WPIS

Assembly information	
Assembly site	Longgang (China)
Package description	TO-220FP
Molding compound	Epoxy Resin
Frame material	Bare Copper
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	2 mils Cu
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Longgang (China)
Tester	IP TEST



D.U.T.: STF20NK50Z LINE: EZ5L PACKAGE: TO-220FP

Wafer/Die fab. information	
Wafer fab manufacturing location	AMK (Singapore)
Technology	Power MOSFET SuperMesh™ Technology
Die finishing back side	Ti/Ni/Au
Die size	6840 x 5060 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	AMK (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Longgang (China)
Package description	TO-220FP
Molding compound	Epoxy Resin
Frame material	Raw Copper - Selected Ni/NiP
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg - 10 mils Al Source Pad
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Longgang (China)
Tester	IP TEST



5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	BUL1203EP	BT07	Power BIPOLAR
2	STP4NK60ZFP	EZ62	Power MOSFET
3	STF20NK50Z	EZ5L	Power MOSFET

5.2 Reliability test plan and results summary

D.U.T.: BUL1203EP LINE: BT07 PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTSL	N	JESD22 A-103	TA=150°C	77	168 H	0/77	
					500 H	0/77	
					1000 H	Running	
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	0/77	
TC	N	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	Running	
TF	N	Mil-Std 750D Method 1037	Δ TC=105°C - Pd=4.8W	20	5 Kcy	0/20	
					10 Kcy	0/20	



D.U.T.: STP4NK60ZFP LINE: EZ62 PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTSL	N	JESD22 A-103	TA=150°C	77	168 H	0/77	
					500 H	0/77	
					1000 H	Running	
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	0/77	
TC	N	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	Running	
TF	N	Mil-Std 750D Method 1037	$\Delta TC=105^{\circ}C$ - Pd=4.8W	20	5 Kcy	0/20	
					10 Kcy	0/20	



D.U.T.: STF20NK50Z LINE: EZ5L PACKAGE: TO-220FP

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
HTSL	N	JESD22 A-103	TA=150°C	77	168 H	0/77	
					500 H	0/77	
					1000 H	Running	
AC	N	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	0/77	
TC	N	JESD22 A-104	TA=-65°C TO +150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	Running	
TF	N	Mil-Std 750D Method 1037	Δ TC=105°C - Pd=4.8W	20	5 Kcy	0/20	
					10 Kcy	0/20	

ANNEXES 6.0

6.1 Tests Description

Test name	Description	Purpose
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF Thermal Fatigue	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.

Qualification of ECOPACK®2 conversion for products in TO-220FPAC/AB packages

General Information	
Product Line	Power Rectifiers (BU78) / AC switches (BU58)
Product Description	Rectifiers / AC switches in TO-220FPAC/AB packages: ECOPACK®2 conversion
Product Group	APM
Product division	ASD & IPAD
Package	TO-220FPAB/TO-220FPAC
Maturity level step	Qualified

Locations	
Wafer fab	STM Tours (France) STM Ang Mo Kio (Singapore)
Assembly plant	ST Shenzhen (China)
Reliability Lab	STM Tours (France)

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	28-Feb-2011	11	I. BALLON	First issue Qualification of Power Rectifiers / AC switches in TO-220FPAC/AB packages: ECOPACK®2 conversion (Reference document: Product Change Notification PCN APM/11/6300)

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
FMEA	FMEA 8250500
RER	1011008

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
UHASt	Unbiased Highly Accelerated Stress Test
THB	Temperature Humidity Bias
TF/IOLT	Thermal Fatigue/Intermittent Operational Life
RSH	Resistance to solder Heat
	Solderability

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to evaluate the reliability of ST products (Power Rectifiers /AC switches) housed in TO-220FPAC/AB packages with the "Halogen-Free" encapsulation molding compound.

According FMEA 8250500, tests vehicles have been chosen covering Power Rectifiers, with largest die size and voltage available in TO-220FPAC/AB packages. Two products AC switches have been chosen regarding bonding configuration and technologies used.

The reliability methodology used in this qualification follows the JESD47-G: «Stress Test Driven Qualification Methodology».

3.2 Conclusion

The perimeter addressed in this campaign qualifies the production of Power Rectifiers and AC switches housed in TO-220FPAC/AB packages with the "Halogen-Free" encapsulation molding compound.

Reliability tests are positive.

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

- Power Rectifiers / AC switches in TO-220FPAC/AB packages in ECOPACK®2 Molding compound.

4.2 Construction note

Power Rectifiers / AC switches in TO-220FP packages in ECOPACK®2 Molding compound	
Wafer/Die fab. information	
Wafer fab manufacturing location	STM Ang Mo Kio (Singapore) STM Tours (France)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	STM Shenzhen (China)
Assembly information	
Assembly site	STM in China
Package description	TO-220FPAC / TO-220FPAB
Molding compound	ECOPACK®2 ("Halogen-free") molding compound
Frame material	Copper
Die attach process	Soft solder
Die attach material	Preform Pb/Sn/Ag
Wire bonding process	Ultra Sonic wire bonding
Wires bonding materials	Aluminium
Lead finishing process	Plating
Lead finishing material	Tin (Sn 100%)
Final testing information	
Testing location	STM in China (Shenzhen)

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Process/ Package	Product Family	Product
1	TO-220FPAB	Power Rectifiers	STPS30M100SFP
2			STPS30H60CFP
3			STTH2002CFP
4	TO-220FPAC		STTH15R06FP
5	TO-220FPAB	AC switches	TYN612MFP
6			ACST210-8FP

5.2 Test plan and results summary

Die Oriented Tests

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 3	Lot 4	
HTRB	N	JESD22 A-108	T _j , V _r = 0.8xV _{rrm}	231	168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
			T _j max, V=VAC peak	SS	Steps	Failure/SS			Note
						Lot 5	Lot 6		
				154	168 H	0/77	0/77		
					500 H	0/77	0/77		
					1000 H	0/77	0/77		


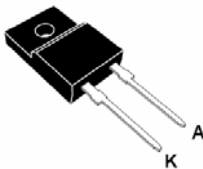
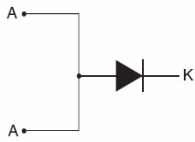
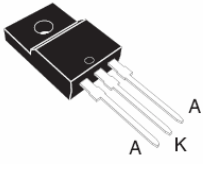

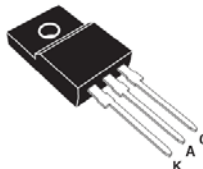
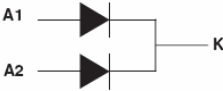
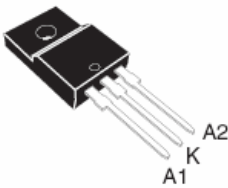
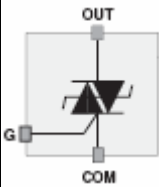
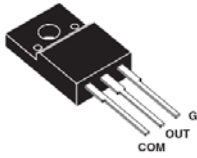
Package Oriented Tests

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 3	Lot 5	
THB	N	JESD22 A-101	T _a = 85°C, RH = 85%, V _r = 0.8xV _{rrm} or 100V max	75	168 H	0/25	0/25	0/25	
					500 H	0/25	0/25	0/25	
					1000 H	0/25	0/25	0/25	
TC	N	JESD22 A-104	T _a = -65°C to 150°C	SS	Steps	Failure/SS			Note
						Lot 4	Lot 5	Lot	
	N			50	100 cy	0/25	0/25		
					500 cy	0/25	0/25		
IOLT	N	MIL-STD 750 Method 1037	IF, delta TC=85°C	75	8572 cycles	Failure/SS			Note
						Lot 3	Lot 4	Lot 6	
uHAST	N	JESD22 A118	130°C, 85%HR, 3 bars	SS	Steps	Failure/SS			Note
						Lot 5			
RSH	N		260°C 10s ON / 15s OFF	SS	Steps	Failure/SS			Note
						Lot 4	Lot 5	Lot 6	
						0/12	0/12	0/12	
Solderability	N	J-STD-002		SS	Steps	Failure/SS			Note
						Lot 1	Lot 4	Lot 5	
						Lot 1	Lot 4	Lot 5	
				40		Failure/SS			Note
						Lot 1	Lot 4	Lot 5	
				40		Failure/SS			Note
						Lot 1	Lot 4	Lot 5	

6 ANNEXES

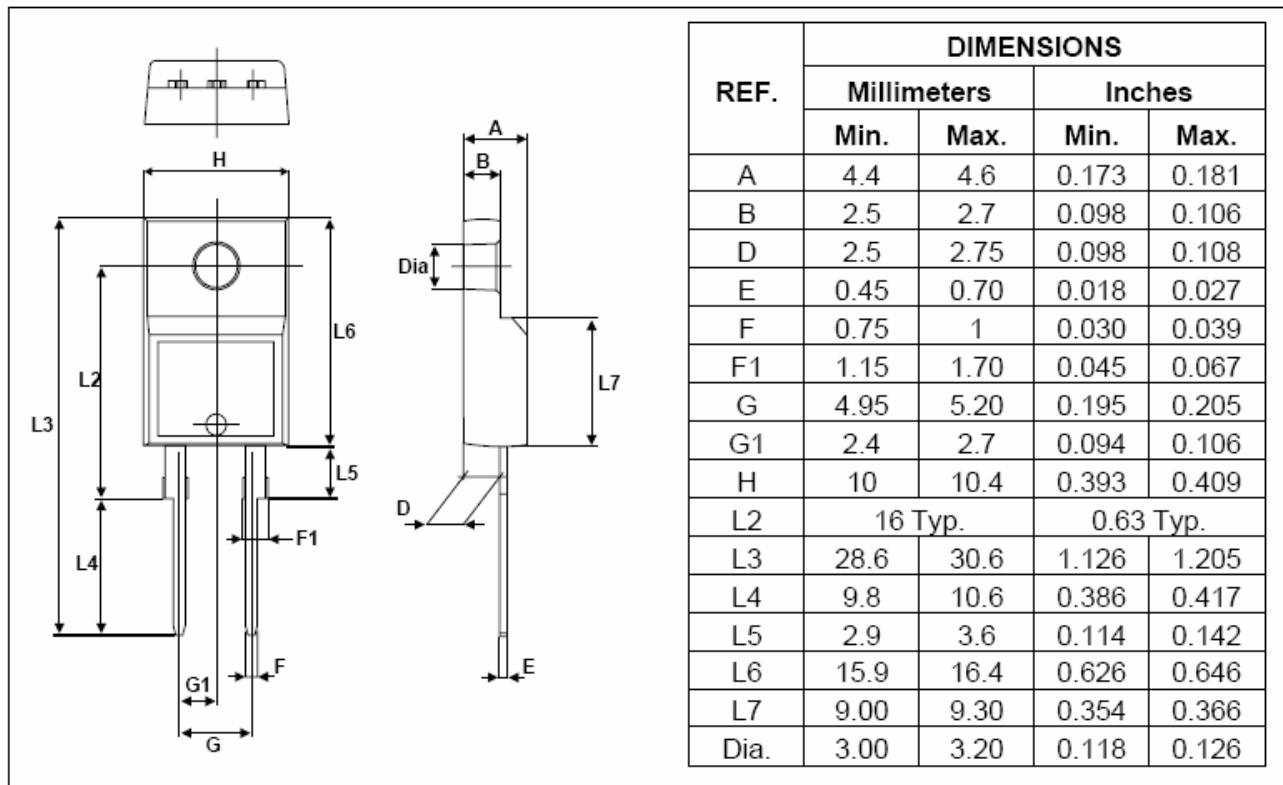
6.1 Device details

6.1.1 Pin connection

Package	Pin connection	
	Power Rectifiers	AC switches
TO-220FPAC	 	N/A
TO-220FPAB	 	 
	 	 

6.1.2 Package outline/Mechanical data

- TO-220FPAC



- TO-220FPAB

Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.4	4.6	0.173	0.181
B	2.5	2.7	0.098	0.106
D	2.5	2.75	0.098	0.108
E	0.45	0.70	0.018	0.027
F	0.75	1	0.030	0.039
F1	1.15	1.70	0.045	0.067
F2	1.15	1.70	0.045	0.067
G	4.95	5.20	0.195	0.205
G1	2.4	2.7	0.094	0.106
H	10	10.4	0.393	0.409
L2	16 Typ.		0.63 Typ.	
L3	28.6	30.6	1.126	1.205
L4	9.8	10.6	0.386	0.417
L5	2.9	3.6	0.114	0.142
L6	15.9	16.4	0.626	0.646
L7	9.00	9.30	0.354	0.366
Dia.	3.00	3.20	0.118	0.126

6.2 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias HTFB / HTGB High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
IOLT	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors), followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Test name	Description	Purpose
Package Oriented		
uHAST	The device is stored in temperature Ta=130°C humidity 85%RH and vapor pressure 3 bars during 96 hours, or equivalent 110°C 85% RH during 264 hours.	The uHAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.
RSH	The device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.



Reliability Plan

AC Switches and Power Rectifiers in TO-220FP package

Capacity extension in ST site of Long-Gang, China

General Information		Locations	
Product Lines	BU58 & 78 (AC Switches & Rectifiers)	Wafer fab	Tours (France) Ang Mo Kio (Singapore)
Product Description	SCRs, Triacs, ACS devices, Power Schottky & Ultrafast Rectifiers in TO-220FP package	Assembly plant	LONG GANG (China)
P/N	ACSxxx-xxFP ACSTxx-xxFP STPSxxxFP STTHxxxFP TxxxT-600FP TYNxxxFP	Reliability Lab	IMS-APM Tours Reliability Lab
Product Group	IMS – APM		
Product division	ASD & IPAD (Application Specific Device & Integrated Passive and Active Devices)		
Package	TO-220FP (Full Pack)		
Maturity level step	Qualification		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	28/02/2011		M. Verchiani/F. Jauffret	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1.1 Objective

Qualifications of Long Gang as Assembly and Testing Location for TO-220FP package.

1.2 Reliability test plan summary

Power Rectifiers in TO-220FP package

P/N	Tests	Conditions	References	Units
STPS30M100SFP	HTRB	$T_j = 150^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$, 1000Hr	JESD22 A-108	77
	PCT	121°C, 2 bars, 100% RH, 96Hr	JESD22 A-102	25
	THB	$T_a=85^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$ up to 100V, 85%RH, 1000Hr	JESD22 A-101	25
	TC	-65°C/+150°C 2 cycles/hours, 500 cy.	JESD22 A-104	25
STPS30H60CFP	IOLT	$\Delta T_c=85^{\circ}\text{C}$, Power On=3.5min, Power Off= 3.5min, 8572 cy.	MIL-STD 750 Meth. 1037	25
	RSH	10s, $T^{\circ}=260^{\circ}\text{C}$	JESD22 B-106	12
	TC	-65°C/+150°C 2 cycles/hours, 500 cy.	JESD22 A-104	25
	Screwing	Torque Force 0.4 to 0.6 N·n	ST Internal Spec 0063378	22
	Solderability	220°C SnPb Dry and Wet Aging 245°C SnAgCu Dry and Wet Aging	JESD22 B-102	20
STTH2003CFP	IOLT	$\Delta T_c=85^{\circ}\text{C}$, Power On=3.5min, Power Off= 3.5min, 8572 cy.	MIL-STD 750 Meth. 1037	25
	RSH	10s, $T^{\circ}=260^{\circ}\text{C}$	JESD22 B-106	12
	TC	-65°C/+150°C 2 cycles/hours, 500 cy.	JESD22 A-104	25
	Screwing	Torque Force 0.4 to 0.6 N·n	ST Internal Spec 0063378	22
	Solderability	220°C SnPb Dry and Wet Aging 245°C SnAgCu Dry and Wet Aging	JESD22 B-102	20
STTH512FP	HTRB	$T_j = 150^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$, 1000Hr	JESD22 A-108	77
	PCT	121°C, 2 bars, 100% RH, 96Hr	JESD22 A-102	25
	THB	$T_a=85^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$ up to 100V, 85%RH, 1000Hr	JESD22 A-101	25
	Solderability	220°C SnPb Dry and Wet Aging 245°C SnAgCu Dry and Wet Aging	JESD22 B-102	20
STPS2045CFPY	HTRB	$T_j = 150^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$, 1000H	JESD22 A-108	77
	IOLT	$\Delta T_c=85^{\circ}\text{C}$, Power On=3.5min, Power Off= 3.5min, 8572 cy.	MIL-STD 750 Meth. 1037	75
	PCT	121°C, 2 bars, 100% RH, 96Hr	JESD22 A-102	77
	RSH	10s, $T^{\circ}=260^{\circ}\text{C}$	JESD22 B-106	12
	TC + DPA	-65°C/+150°C 2 cycles/hours, 1000 cycles	JESD22 A-104	77
	Screwing	Torque Force 0.4 to 0.6 N·n	ST Internal Spec 0063378	22
	THB	$T_a=85^{\circ}\text{C}$, $V=0.8 \times \text{VRRM}$ up to 100V, 85%RH, 1000Hr	JESD22 A-101	77



AC Switches in TO-220FP package

Test Vehicle	HTRB	TC	UHASt	Stalled Rotor test*	Construction analysis
TYN612MFP	1 lot (77 pcs)	1 lot (25 pcs)	1 lot (25 pcs)	n/a	3 pcs
ACST1035-7FP	1 lot (77 pcs)	1 lot (25 pcs)	1 lot (25 pcs)	1 lot (25 pcs)	3 pcs

(*) Stalled Rotor Test conditions:

Ton = 8 sec.
Toff = 90 sec.
I peak = 11.3A.
Tamb = 25°C
DeltaTc = 91°C and DeltaTj = 150°C
Sample size: 25 pieces ACST10-7SFP.
Duration: 10 Kcycles
Expected results: no failure over 25 units

1.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias HTFB / HTGB High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.



Test name	Description	Purpose
IOLT	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
UHASt	The device is stored in temperature Ta=130°C humidity 85%RH and vapor pressure 3 bars during 96 hours, or equivalent 110°C 85% RH during 264 hours.	The uHASt is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
RSH	The device is submitted to a dipping in a solder bath at 260°C with a dwell time of 10s. Only for through hole mounted devices.	This test is used to determine whether solid state devices can withstand the effects of the temperature to which they will be subjected during soldering of their leads. The heat is conducted through the leads into the device package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

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