


**PRODUCT / PROCESS CHANGE NOTIFICATION**

**1. PCN basic data**

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.	MICROCONTROLLERS/24/14922	
1.3 Title of PCN	JSCC (China) LQFP7x7 48L , LQFP10x10 64L and UFQFPN7X7 48L new BOM for STM32H523x and STM32H533x listed product.	
1.4 Product Category	STM32H523xx & STM32H533xx	
1.5 Issue date	2024-08-18	

**2. PCN Team**

<b>2.1 Contact supplier</b>	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
<b>2.2 Change responsibility</b>	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

**3. Change**

<b>3.1 Category</b>	<b>3.2 Type of change</b>	<b>3.3 Manufacturing Location</b>
Materials	Direct Material: Bond Wire - Metallurgy (metallic composition/ raw material)	StatsChipPAC JSCC Jiangyin China

**4. Description of change**

	<b>Old</b>	<b>New</b>
4.1 Description	Assembly lines / wire bonding: - JSCC (China) / Gold wire	Assembly lines / wire bonding: - JSCC (China) / Copper Palladium wire additional source - JSCC (China) / Gold wire
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No change in Form, no change in Fit, no change in Function. Package darkness might change depending on molding compound. Pin1 identifier remain in the same corner but might slightly change in terms of form and positioning.	

**5. Reason / motivation for change**

5.1 Motivation	Due to the success on the market of STM32 devices, ST Microcontrollers Division decided to qualify an additional back-end assembly line to maintain state of the art service level to our customers thanks to extra capacity.
5.2 Customer Benefit	SERVICE IMPROVEMENT

**6. Marking of parts / traceability of change**

6.1 Description	Traceability ensure by ST internal tools
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**7. Timing / schedule**

7.1 Date of qualification results	2024-08-05
7.2 Intended start of delivery	2024-11-01
7.3 Qualification sample available?	Upon Request

**8. Qualification / Validation**

8.1 Description	14922 PCN14922_Reliability RER2220 and RER2321.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-08-18

9. Attachments (additional documentations)
14922 Public product.pdf 14922 PCN14922_Reliability RER2220 and RER2321.pdf 14922 PCN14922_Additional information.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STM32H523CET6	
	STM32H523CEU6	
	STM32H523RET6	
	STM32H533CET6	
	STM32H533CEU6	
	STM32H533RET6	

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## PRODUCT/PROCESS CHANGE NOTIFICATION

### PCN14922 – Additional information

**JSCC (China) LQFP7x7 48L, LQFP10x10 64L and UFQFPN7X7 48L new BOM for STM32H523x and STM32H533x listed product.**

#### MDRF – General Purpose Microcontrollers Division (GPM)

##### What are the changes?

Introduction of an additional assembly line to continue our path through the deployment of our Low-cost wire strategy to secure our supply chain.

Changes are described in table below:

	Existing back-end assembly line	Added assembly line
Assembly site	StatsChipPAC JSCC Jiangyin China	
package	UFQFPN7X7 48L	
Wire bonding	Gold 0.8Mils	CuPd 0.8Mils

package	LQFP7x7 48L & LQFP10x10 64L	
Glue	D/A Ablestik 3230	HITACHI EN4900GC
Molding compound <sup>(1)</sup>	SUMITOMO G631SHQ	SUMITOMO G700LALA
Wire bonding	Gold 0.8Mils	CuPd 0.8Mils

(1) Package darkness might change depending on molding compound. The visual aspect (color) might change depending on substrate material. Marking position and size could be different upon assembly site, without any loss of information.

##### How can the change be seen?

The standard marking is not changing : Traceability ensured by ST internal tools  
Please refer to Technical Note **TN1433** for package marking details.

## How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number “**PCN14922**” into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request

Partial Ship: 01 Price Pol: 05 Status: 01 Canc:

%: 0 Sample Type: Sample Non Std Type

Closing Type: Sample Std Type  
Sample Non Std Type  
Sample Non Std w Spl Tests

Lab Sheet:

SO | NPO Sample

Header

SO Nr: 8018502433 Customer: 99770200 01 ST-TOKYO SO Type: 30 Sample Order Cost Center: JT3129 SAMPLES /SALES J

PO Nr: Carrier Code: 0001 Price Policy: 05 Currency: 02 U.S. DOLLAR Req Name:

Notes: Status: 01 All items pending,ni Issuing Date: 25-JUN-2018 Ord Val: 0.0000 Sample Req Date: 25-Jun-2018

Sch I Nr	PO I. Nr.	Finished Good	Comm Qty	Open Qty	Plant Open Qty	Reqd Qty	Unit Price	RD	CD	EDD	St
1.1.10	000001	STM32F429NIH6	30	30	30	30	0.0000	25-Jun-18	01-Mar-59	01-Mar-59	01

Final Cust: PO Item: 000001 Comm Prod: STM32F429NIH6 Qty: 30 RD: 25-Jun-18 Unit Price: 0.0000 Final Cust: 8800367006 SANSHIN/NPC

Cust Part Nr: Finished Good: Partial Ship: 01 Price Pol: 05 Status: 01 Canc:

Notes: TAM K Pieces: 0 Our Share%: 0 Sample Type: Sample Non Std Type

Project Name: Closing Date: Closing Type:

Regional Sheet: **PCN 14922** Lab Sheet:

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**JSCC (China) LQFP7x7 48L, LQFP10x10 64L and UFQFPN7X7 48L new BOM for STM32H523x and STM32H533x listed product.**

**MDRF – General Purpose Microcontrollers Division (GPM)**

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**MDRF-GPM-RER2220**

JSCC (China) additional source in UFQFPN 5X5 32L, UFQFPN 7X7 48L and VFQFPN 8x8 68L

PCN14068 – PCN14922

General Information		Traceability	
Commercial Product	STM32G031K8U6, STM32G071CBU6, STM32H503CBU6, STM32U535CEU6	Diffusion Plant	TSMC Fab14, Crolles 300
Product Line	466X66, 460X66, 474X66, 455X66	Assembly Plant	SC-StatsChippac-China (JSCC)
Die revision	466: Cut1.2, 460: Cut2.1, 474: Cut1.2, 455: Cut1.1	Reliability Assessment	
Package	UFQFPN 7X7X0.55 48L 0.5 MM PITCH, UFQFPN 5X5X0.55 32L 0.5 MM PITCH		
Silicon Technology	TN090C, CMOSE40ULP, TN040CE		
Division	MDRF-GPM	Pass	<input checked="" type="checkbox"/>
		Fail	

Release	Date	Author	Function
1.0	12/02/2024	Céline Navarro	GPM BE Q&R
2.0	05/08/2024	Gabin Bosco	GPM BE Q&R

**DOCUMENT ACTORS:**

Release	Name	Function	Location	Date
1.0	Pascal NARCHE	Subgroup Quality Manager	Rousset	27/3/2024
	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	27/3/2024
2.0	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	05/8/2024

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**MDRF-GPM-RER2321**

JSCC (China) LQFP7x7 32L/48L, LQFP10x10 64L and LQFP12x12 80L package copper palladium bonding wire introduction on STM32 listed products

PCN14363 – PCN14922

General Information		Traceability	
Commercial Product	QC32G030K6T6, QC32H503RBT6, QC32H562RGT6, QC32G081MBT6, QC32G414CBT6, QC32U535RBT6	Diffusion Plant	TSMC Fab14 DIFF, Crolles 300
Product Line	466X66, 474X66, 484X66, 467X66, 469X66, 455X66	Assembly Plant	SC-StatsChippac-China (JSCC)
Die revision	cut1.2, cut1.2, cut1.3, cut1.1, cut2.3, cut1.1	Reliability Assessment	
Package	LQFP 32 7x7x1.4, LQFP 64 10x10x1.4, LQFP 80 12x12x1.4, LQFP 48 7x7x1.4		
Silicon Technology	TN090CE, CMOSE40ULP, TN040CE		
Division	MDRF-GPM	Pass	<input checked="" type="checkbox"/>
		Fail	

Release	Date	Author	Function
1.0	17/05/2024	Céline Navarro	GPM BE Q&R
		Gabin Bosco	
2.0	27/06/2024	Gabin Bosco	GPM BE Q&R
3.0	05/08/2024	Gabin Bosco	GPM BE Q&R

See next page



## Reliability Report

### MDRF-GPM-RER2220

JSCC (China) additional source in UFQFPN 5X5 32L, UFQFPN 7X7 48L and VFQFPN 8x8 68L

PCN14068 – PCN14922

General Information	
Commercial Product	STM32G031K8U6, STM32G071CBU6, STM32H503CBU6, STM32U535CEU6
Product Line	466X66, 460X66, 474X66, 455X66
Die revision	466: Cut1.2, 460: Cut2.1, 474: Cut1.2, 455: Cut1.1
Package	UFQFPN 7X7X0.55 48L 0.5 MM PITCH, UFQFPN 5X5X0.55 32L 0.5 MM PITCH
Silicon Technology	TN090C, CMOSE40ULP, TN040CE
Division	MDRF-GPM

Traceability	
Diffusion Plant	TSMC Fab14, Crolles 300
Assembly Plant	SC-StatsChippac-China (JSCC)

Reliability Assessment	
Pass	<input checked="" type="checkbox"/>
Fail	<input type="checkbox"/>

Release	Date	Author	Function
1.0	12/02/2024	Céline Navarro	GPM BE Q&R
2.0	05/08/2024	Gabin Bosco	GPM BE Q&R

### DOCUMENT ACTORS:

Release	Name	Function	Location	Date
1.0	Pascal NARCHE	Subgroup Quality Manager	Rousset	27/3/2024
	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	27/3/2024
2.0	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	05/8/2024

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## RELIABILITY EVALUATION OVERVIEW

### • OBJECTIVE

The aim of this report is to present the reliability evaluation performed for qualification of copper wires on JSCC (China) UFQFPN 5X5 32L, UFQFPN 7X7 48L packages in TSMC 90nm, Crolles E40 and TSMC N40.

PCN 14068 changes, for listed products, are described in table below:

UFQFPN 5X5 32L		Existing back-end assembly line		New assembly line
Assembly site		ASE Taiwan	StatsChipPAC JSCC Jiangyin China	
Lead frame		Copper Frame Double Ring Ag Plating	HD Copper Frame Ag Plating	
Die Attach		Hitachi EN4900G	ABLEBOND 8290	HITACHI EN4900GC
Molding compound <sup>(1)</sup>		Sumitomo EME-G631H	SUMITOMO G770	SUMITOMO G700LALA
Wire bonding		Gold 0.8Mils	Gold 0.8Mils	CuPd 0.8Mils

UFQFPN 7X7 48L		Existing back-end assembly line		New assembly line
Assembly site		ASE Taiwan	StatsChipPAC JSCC Jiangyin China	
Lead frame		Copper Frame Double Ring Ag Plating	STD Copper Frame Ag Plating	HD Copper Frame Ag Plating
Die Attach		Hitachi EN4900G	ABLEBOND 8290	HITACHI EN4900GC
Molding compound <sup>(1)</sup>		Sumitomo EME-G631H	SUMITOMO G770	SUMITOMO G700LALA
Wire bonding		Gold 0.8Mils		CuPd 0.8Mils

VFQFPN 8X8 68L		Existing back-end assembly line		New assembly line
Assembly site		StatsChipPAC JSCC Jiangyin China		
Lead frame		STD Copper Frame Ag Plating		
Die Attach		HITACHI EN4900GC		
Molding compound /Resin <sup>(1)</sup>		SUMITOMO G770		SUMITOMO G700LALA
Wire bonding		Gold 0.8Mils		CuPd 0.8Mils

(1) Package darkness might change depending on molding compound. Visual aspect (color) might change depending on substrate material. Marking position and size could be different upon assembly site, without any loss of information.

PCN 14922 changes, for added STM32H523x and STM32H533x, are described in table below:

	Existing back-end assembly line	Added assembly line
Assembly site	StatsChipPAC JSCC Jiangyin China	
package	UFQFPN7X7 48L	
Wire bonding	Gold 0.8Mils	CuPd 0.8Mils

## • CONCLUSION

All reliability tests have been completed with positive results for UFQFPN 5X5 32L, UFQFPN 7X7 48L packages. Neither functional nor parametric rejects were detected at final electrical testing.

Package oriented tests have not put in evidence any criticality. Physical analysis performed on samples submitted to tests has not put in evidence any issue. ESD CDM are in accordance with ST spec.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for all product with same silicon technology (TSMC 90nm, Crolles E40 and TSMC N40) as Test vehicles in UFQFPN 5X5 32L, UFQFPN 7X7 48L packages with copper wires in JSCC (China) assembly line.

Refer to section 3.0 for reliability test results

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## Reliability Report

## 1. RELIABILITY STRATEGY

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 specification, in full compliancy with the JESD-47 international standard.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3

## 2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

### 2.1. Generalities

Package line	Device (partial Rawline Code)	Diffusion list	Number of lots
UFQFPN 5x5	61MG*466QCXY	TSMC Fab14	1
UFQFPN 7x7	60MI*460QCXB	TSMC Fab14	2
UFQFPN 7x7	60MI*474QCXY	Crolles 300	1
UFQFPN 7x7	61MI*455QCXZ	TSMC Fab14	1

### 2.2. Traceability

#### 2.2.1. Wafer Fab Information

##### Die 466

Wafer Fab Information		
FAB1		
Wafer fab name / location	TSMC Taiwan / TSMC Fab14 DIFF	
Wafer diameter (inches)	12	
Wafer thickness (µm)	775±25µm	
Silicon process technology	TN090CE	
Number of masks	45	
Die finishing front side (passivation) materials	USG + NITRID Thickness	
Die finishing back side Materials	RAW SILICON	
Die area (Stepping die size)	4.0921 mm² (1889.6µm, 2165.6µm)	
Die pad size	Geometry	Open(X,Y)
	Rectangular	123,59 µm
	Rectangular	65,59 µm
Sawing street width (X, Y) (µm)	80,80	

## Reliability Report

Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	TaN/Ta/CuSeed/Cu	0.240 µm
	2	TaN/Ta/CuSeed/Cu	0.310 µm
	3	TaN/Ta/CuSeed/Cu	0.310 µm
	4	TaN/Ta/CuSeed/Cu	0.310 µm
	5	TaN/Ta/CuSeed/Cu	0.310 µm
	6	TaN/Ta/CuSeed/Cu	0.850 µm
	7	AlCu	1.450 µm

## Die 460

Wafer Fab Information			
FAB1			
Wafer fab name / location	TSMC Taiwan Fab14 DIFF		
Wafer diameter (inches)	12		
Wafer thickness (µm)	775±25µm		
Silicon process technology	TN090CE		
Number of masks	45		
Die finishing front side (passivation) materials	USG + NITRIDE		
Die finishing back side Materials	RAW SILICON		
Die area (Stepping die size)	5.8239 mm² (2326.6µm, 2503.2µm)		
Die pad size	Geometry	Open(X,Y)	
	Rectangular	65,59 µm	
	Rectangular	123,59 µm	
Sawing street width (X, Y) (µm)	79.92,79.84		
Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	TaN/Ta/CuSeed/Cu	0.24 µm
	2	TaN/Ta/CuSeed/Cu	0.31 µm
	3	TaN/Ta/CuSeed/Cu	0.31 µm
	4	TaN/Ta/CuSeed/Cu	0.31 µm
	5	TaN/Ta/CuSeed/Cu	0.31 µm
	6	TaN/Ta/CuSeed/Cu	0.85 µm
	7	AlCu	1.45 µm

## Reliability Report

## Die 455

Wafer Fab Information			
FAB1			
Wafer fab name / location	TSMC Taiwan Fab14 DIFF		
Wafer diameter (inches)	12		
Wafer thickness (µm)	775±25µm		
Silicon process technology	TN040CE		
Number of masks	48		
Die finishing front side (passivation) materials	Oxide + Nitride		
Die finishing back side Materials	RAW SILICON		
Die area (Stepping die size)	11.604 mm² (3406.4µm,3406.4µm)		
Die pad size	Geometry		Open(X,Y)
	Rectangular		65,59 µm
	Rectangular		123,59 µm
Sawing street width (X, Y) (µm)	79.92,79.84		
Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	Cu	0.125 µm
	2	Cu	0.145 µm
	3	Cu	0.145 µm
	4	Cu	0.145 µm
	5	Cu	0.145 µm
	6	Cu	0.850 µm
	7	Cu	3.500 µm
	8	Al	1.500 µm

## Reliability Report

## Die 474

Wafer Fab Information			
FAB1			
Wafer fab name / location	Crolles 300 France		
Wafer diameter (inches)	12		
Wafer thickness (μm)	775±25μm		
Silicon process technology	CMOSE40ULP		
Number of masks	51		
Die finishing front side (passivation) materials	PSG + NITRIDE		
Die finishing back side Materials	RAW SILICON		
Die area (Stepping die size)	5.320 mm² (2352μm, 2262μm)		
Die pad size	Geometry		Open(X,Y)
	Other		54.9,54.9 μm
Sawing street width (X, Y) (μm)	80,80		
Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	TaN/Ta/CuSeed/Cu	0.110 μm
	2	TaN/Ta/CuSeed/Cu	0.140 μm
	3	TaN/Ta/CuSeed/Cu	0.140 μm
	4	TaN/Ta/CuSeed/Cu	0.140 μm
	5	TaN/Ta/CuSeed/Cu	0.140 μm
	6	TaN/Ta/CuSeed/Cu	0.850 μm
	7	TaN/Ta/CuSeed/Cu	0.850 μm
	8	Ta/TaN/AlCu	1.525 μm

### 2.2.2.Assembly Information

Assembly Information	
Package 1:UFQFPN 7X7X0.55 48L 0.5 MM PITCH	
Assembly plant name / location	STATSChipPAC-China JSCC
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25µm
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	UQFN7x7 48L HD Sn 5.2mmSq
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm
Die attach material/type(glue/film)/supplier	Glue EN4900GC Hitachi
Wire bonding material/diameter	Wire CuPd 0.8 mils
Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
Package 2:UFQFPN 5X5X0.55 32L 0.5 MM PITCH	
Assembly plant name / location	STATSChipPAC-China JSCC
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25µm
Die sawing method	Laser groove + mechanical sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	UQFN5x5 32L HD Sn 3.1mmSq
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm
Die attach material/type(glue/film)/supplier	Glue EN4900GC Hitachi
Wire bonding material/diameter	Wire CuPd 0.8 mils
Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

### 2.2.3. Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDRF Rel Lab , JSCC Rel Lab, Muar BE lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: [http://www.st.com/content/st\\_com/en/support/quality-and-reliability/certifications.html](http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html)

## 3. TEST RESULTS SUMMARY

If the test plan is not in line with the one planned initially, include necessary explanation.

### 3.1. Lot information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	9R318264	Cut 1.2	GQ33824E	64MI*466QCXY	UFQFPN 5X5X0.55 32L	
Lot 2	9R306165	Cut 2.1	GQ338217	60MI*460QCXB	UFQFPN 7X7X0.55 48L	
Lot 3	9R306165	Cut 2.1	GQ338217	60MI*460QCXB	UFQFPN 7X7X0.55 48L	
Lot 4	VQ237956	Cut 1.2	GQ347263	60MI*474QCXY	UFQFPN 7X7X0.55 48L	
Lot 5	9R237233	Cut 1.1	GQ34926L	61MI*455QCXZ	UFQFPN 7X7X0.55 48L	

## Reliability Report

### 3.2. Test plan and results summary

#### ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	JSTD 020 JESD 22-A113	24h bake@125°C, MSL3 (192h/30°C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	4	308	1232	Lot 2: 0/308 Lot 3: 0/308 Lot 4: 0/308 Lot 5: 0/308	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs <input checked="" type="checkbox"/> After PC	4	77	308	Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	
TC	JESD22-A104	Ta= -65 to 150°C Cyc= 500 cy <input checked="" type="checkbox"/> After PC	4	77	308	Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	
THB	JESD22-A101	Ta= 85%HR/85°C/VDD max Duration= 1000hrs <input checked="" type="checkbox"/> After PC	4	77	308	Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	
UHASt	JESD22-A118	Ta= 130°C/85%RH Duration= 96hrs <input checked="" type="checkbox"/> After PC	4	77	308	Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77	

#### ELECTRICAL VERIFICATION TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CDM	JEDEC JS-002	Voltage= 500V for die 466 500V for die 460 500V for die 474 500V for die 455 except pin PC15 250V	4	3		Lot 1: 0/3 Lot 2: 0/3 Lot 4: 0/3 Lot 5: 0/3	

#### PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CA	JESD 22B102 JESD B100/ B108 ST internal specifications	Construction analysis including POA Solderability and BS/PT	5	50	250	Lot 1: 0/50 Lot 2: 0/50 Lot 3: 0/50 Lot 5: 0/50	NRL202310_0094 NRL202310_0064 MDG_Muar_23_00060 NRL202312_0382

Note: Test method revision reference is the one active at the date of reliability trial execution.

#### 4. APPLICABLE AND REFERENCE DOCUMENTS

Remove from below list not applicable documents.

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A101	Temperature Humidity Bias
JESD 22B102	Solderability test
JESD B100/ B108	Physical dimension

#### 5. GLOSSARY

CDM	Electrostatic Discharge - Charged device model
THB	Temperature Humidity Bias
CA	Construction analysis System
HTSL	HTSL Storage Life High temperature storage life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHASt	Unbiased HAST (Highly Accelerated Stress Test)
DMS	ST Advanced Documentation Controlled system/ Documentation Management System

#### 6. REVISION HISTORY

Release	Date	Description
1.0	12/02/2024	Initial Release
2.0	05/08/2024	PCN14922 added

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## Reliability Report

### MDRF-GPM-RER2321

JSCC (China) LQFP7x7 32L/48L, LQFP10x10 64L and LQFP12x12 80L package copper palladium bonding wire introduction on STM32 listed products

PCN14363 – PCN14922

General Information	
Commercial Product	QC32G030K6T6, QC32H503RBT6, QC32H562RGT6, QC32G0B1MBT6, QC32G414CBT6, QC32U535RBT6
Product Line	466X66, 474X66, 484X66, 467X66, 469X66, 455X66
Die revision	cut1.2, cut1.2, cut1.3, cut1.1, cut2.3, cut1.1
Package	LQFP 32 7x7x1.4, LQFP 64 10x10x1.4, LQFP 80 12X12X1.4, LQFP 48 7x7x1.4
Silicon Technology	TN090CE, CMOSE40ULP, TN040CE
Division	MDRF-GPM

Traceability	
Diffusion Plant	TSMC Fab14 DIFF, Crolles 300
Assembly Plant	SC-StatsChippac-China (JSCC)

Reliability Assessment	
Pass	<input checked="" type="checkbox"/>
Fail	

Release	Date	Author	Function
1.0	17/05/2024	Céline Navarro Gabin Bosco	GPM BE Q&R
2.0	27/06/2024	Gabin Bosco	GPM BE Q&R
3.0	05/08/2024	Gabin Bosco	GPM BE Q&R

### DOCUMENT ACTORS:

Release	Name	Function	Location	Date
1.0	Pascal NARCHE	Subgroup Quality Manager	Rousset	20/05/2024
	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	20/05/2024
2.0	Pascal NARCHE	Subgroup Quality Manager	Rousset	27/06/2024
3.0	Berengere ROUTIER-SCAPPUCCI	GPM BE Q&R Manager	Rousset	5/08/2024

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## RELIABILITY EVALUATION OVERVIEW

### • OBJECTIVE

The aim of this report is to present the reliability evaluation performed for qualification of copper wires on JSCC (China) LQFP7x7 32L/48L, LQFP10x10 64L and LQFP12x12 80 packages in TSMC 90nm, Crolles 40nm and TSMC 40nm.

PCN 14363 changes, for STM32C0x, STM32G0/G4x, STM32H5/H7x, STM32L4/L5x and STM32U5x are described in table below:

	Existing back-end line				Added back-end line
Assembly site	ASE		StatsChipPAC JSCC Jiangyin (China)		
Molding Compound	Sumitomo EME-G631SH		Sumitomo EME-G631SHQ		Sumitomo EME-G700LA type LA
GLUE	SUMITOMO EPOXY CRM 1076WA	HITACHI EN4900G	Die Attach Loctite Ablestik 3230		HITACHI EN4900GC
Wire	Gold 2N 0.8mil	Copper Palladium 0.8mil	Gold 0.8mil	Silver 96.5% 0.8mil	Copper Palladium 0.8mil
Marking composition	Without 2D	With 2D Marking	Without 2D		With 2D Marking
PP code on marking	AA		GQ		

PCN 14922 changes, for added STM32H523x and STM32H533x, are described in table below:

	Existing back-end assembly line	Added assembly line
package	<b>LQFP7x7 48L &amp; LQFP10x10 64L</b>	
Glue	D/A Ablestik 3230	HITACHI EN4900GC
Molding compound <sup>(1)</sup>	SUMITOMO G631SHQ	SUMITOMO G700LALA
Wire bonding	Gold 0.8Mils	CuPd 0.8Mils

(1) Package darkness might change depending on molding compound. The visual aspect (color) might change depending on substrate material. Marking position and size could be different upon assembly site, without any loss of information.

- **CONCLUSION**

All reliability tests have been completed with positive results for LQFP7x7 32L/48L, LQFP10x10 64L and LQFP12x12 80L packages. Neither functional nor parametric rejects were detected at final electrical testing.

Package oriented tests have not put in evidence any criticality. Physical analysis performed on samples submitted to tests has not put in evidence any issue. ESD CDM are in accordance with ST spec.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for all products with same silicon technology (TSMC 90nm, Crolles E40) as Test vehicles in LQFP7x7 32L/48L, LQFP10x10 64L and LQFP12x12 80L packages with copper wires in JSCC (China) assembly line. TSMC N40 technology will be qualified on Q3'2024.

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## 1. RELIABILITY STRATEGY

Reliability strategy and test vehicles choice defined upon risk analysis and product matrix showing criticalities of packages with backlog volumes.

Reliability lots have been defined as below to cover technologies and assembly line qualification. All technologies with qualification granted on the assembly line directly qualify all associated products:

- 3 lots of TSMC N90 for technology and JSCC LQ copper assembly line qualification
- 2 lots of Crolles E40 for technology qualification on JSCC LQ copper assembly line. 2 lots to cover bonding specificities
- 1 lot of TSMC N40 for technology qualification on JSCC LQ copper assembly line

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 specification, in full compliancy with the JESD-47 international standard.

For details on test conditions and specifications references, refer to test results summary in section 3

## 2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

### 2.1. Generalities

Package line	Device (partial Rawline Code)	Diffusion list	Number of lots
LQFP 32 7x7	645V*466QCXY	TSMC Fab14	1
LQFP 64 10x10	605W*474QCXY	Crolles 300	1
LQFP 64 10x10	625W*484QCXX	Crolles 300	1
LQFP 80 12X12	649X*467QCXZ	TSMC Fab14	1
LQFP 48 7x7	6H5B*469QCXX	TSMC Fab14	1
LQFP 64 10x10	665W*455QCXZ	TSMC Fab14	1

### 2.2. Traceability

#### 2.2.1. Wafer Fab Information

##### Die – 474 - 484

Wafer Fab Information		
FAB1	Die 474	Die 484
Wafer fab name / location	Crolles 300 / Crolles 300 12	
Wafer diameter (inches)	12	
Wafer thickness (µm)	775±25µm	
Silicon process technology	CMOSE40ULP	
Number of masks	51	
Die finishing front side (passivation) materials	PSG NITRIDE	
Die finishing back side Materials	RAW SILICON	
Die area (Stepping die size)	Die 474 5.320 mm <sup>2</sup> (2352, 2262)	Die 484 11.60 mm <sup>2</sup> (3518, 3297)

Die pad size	54.9,54.9 µm		
Sawing street width (X,Y) (µm)	80,80		
Metal levels/Materials/Thicknesses	<b>Wire bond pad metal</b>	<b>Composition</b>	<b>Thickness</b>
	1	TaN/Ta/CuSeed/Cu	0.11 µm
	2	TaN/Ta/CuSeed/Cu	0.14 µm
	3	TaN/Ta/CuSeed/Cu	0.14 µm
	4	TaN/Ta/CuSeed/Cu	0.14 µm
	5	TaN/Ta/CuSeed/Cu	0.14 µm
	6	TaN/Ta/CuSeed/Cu	0.85 µm
	7	TaN/Ta/CuSeed/Cu	0.85 µm
	8	Ta/TaN/AlCu	1.525 µm

### Die – 467 - 469 - 466

Wafer Fab Information				
FAB1	Die 467		Die 469	Die 466
Wafer fab name / location	TSMC Taiwan / Fab14 DIFF			
Wafer diameter (inches)	12			
Wafer thickness (µm)	775±25µm			
Silicon process technology	TN090CE			
Number of masks	45	43		45
Die finishing front side (passivation) materials	USG NITRIDE			
Die finishing back side Materials	RAW SILICON			
Die area (Stepping die size)	9.969 mm² (3125, 3190.2)	17.390 mm² (4298.4, 4045.6)		4.0921 mm² (1889.6, 2165.6)
Die pad size	Geometry	Die467 Open(X,Y)	Die469 Open(X,Y)	Die466 Open(X,Y)
	Rectangular	65,59 µm	123,59 µm	65,59 µm
	Rectangular	123,59 µm		123,59 µm
Sawing street width (X,Y) (µm)	80,80			

Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	TaN/Ta/CuSeed/Cu	0.24 $\mu\text{m}$
	2	TaN/Ta/CuSeed/Cu	0.31 $\mu\text{m}$
	3	TaN/Ta/CuSeed/Cu	0.31 $\mu\text{m}$
	4	TaN/Ta/CuSeed/Cu	0.31 $\mu\text{m}$
	5	TaN/Ta/CuSeed/Cu	0.31 $\mu\text{m}$
	6	TaN/Ta/CuSeed/Cu	0.85 $\mu\text{m}$
	7	AlCu	1.45 $\mu\text{m}$

## Die – 455

Wafer Fab Information			
FAB1	Die 455		
Wafer fab name / location	TSMC Taiwan / Fab14 DIFF		
Wafer diameter (inches)	12		
Wafer thickness ( $\mu\text{m}$ )	775 $\pm$ 25 $\mu\text{m}$		
Silicon process technology	TN040CE		
Number of masks	48		
Die finishing front side (passivation) materials	OXIDE+NITRIDE		
Die finishing back side Materials	RAW SILICON		
Die area (Stepping die size)	3406.4,3406.4		
Die pad size	Geometry		Open(X,Y)
	Rectangular		54.9,55.38 $\mu\text{m}$
	Square		54.9,54.9 $\mu\text{m}$
Sawing street width (X,Y) ( $\mu\text{m}$ )	80,80		
Metal levels/Materials/Thicknesses	Wire bond pad metal	Composition	Thickness
	1	Cu	0.125 $\mu\text{m}$
	2	Cu	0.145 $\mu\text{m}$
	3	Cu	0.145 $\mu\text{m}$
	4	Cu	0.145 $\mu\text{m}$
	5	Cu	0.145 $\mu\text{m}$
	6	Cu	0.85 $\mu\text{m}$
	7	Cu	3.500 $\mu\text{m}$
	8	Al	1.500 $\mu\text{m}$

## 2.2.2.Assembly Information

Assembly Information			
Package 1: LQFP 32 7x7x1.4			
Assembly plant name / location	StatsChippac-China (JSCC)		
Pitch (mm)	0.8		
Die thickness after back-grinding (µm)	375+/-25µm		
Die sawing method	Laser groove + mechanical cut		
Bill of Material elements			
Lead frame/Substrate material/supplier/reference	LQ7 32L 210sq no slots STMP LF		
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm		
Die attach material/glue/supplier	Hitachi EN4900GC		
Wire bonding material/diameter	CuPd 0.8 mils		
Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA		
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3		
Package 2: LQFP 64 10x10x1.4	Die 474	Die 484	Die 455
Assembly plant name / location	StatsChippac-China (JSCC)		
Pitch (mm)	0.5		
Die thickness after back-grinding (µm)	375+/-25µm		
Die sawing method	Laser groove + mechanical cut		
Bill of Material elements			
Lead frame/Substrate material/reference	LQ10 64L 157Eff noslot MHT	LQ10 64L 207sq Eff slots STMP	LQ10 64L 207sq Eff slots STMP
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm		
Die attach material/glue/supplier	Hitachi EN4900GC		
Wire bonding material/diameter	CuPd 0.8 mils		
Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA		
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3		
Package 3: LQFP 80 12X12X1.4			
Assembly plant name / location	StatsChippac-China (JSCC)		
Pitch (mm)	0.5		
Die thickness after back-grinding (µm)	375+/-25µm		
Die sawing method	Laser groove + mechanical cut		
Bill of Material elements			
Lead frame/Substrate material/reference	LQ12 80L 208sq eff slot Etch LF		
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm		
Die attach material/glue/supplier	Hitachi EN4900GC		
Wire bonding material/diameter	CuPd 0.8 mils		

Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3
<b>Package 4: LQFP 48 7x7x1.4</b>	
Assembly plant name / location	StatsChippac-China (JSCC)
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375+/-25µm
Die sawing method	Laser groove + mechanical cut
<b>Bill of Material elements</b>	
Lead frame/Substrate material/reference	LQFP48L 184sq Eff slots pur tin STMP LF
Lead frame finishing (material/thickness)	Pure Tin (e3) - Tolerance 7 to 20 µm
Die attach material/glue/supplier	Hitachi EN4900GC
Wire bonding material/diameter	CuPd 0.8 mils
Molding compound material/supplier/reference	RESIN SUMITOMO G700LALA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	3

### 2.2.3. Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, Rousset MDRF Rel Lab, JSCC Rel Lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: [http://www.st.com/content/st\\_com/en/support/quality-and-reliability/certifications.html](http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html)

## 3. TEST RESULTS SUMMARY

### 3.1. Lot information

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
Lot 1	9R319028	cut1.2	GQ34429C	645V*466QCXY	LQFP 32 7x7x1.4	
Lot 2	VQ237956	cut1.2	GQ405265	605W*474QCXY	LQFP 64 10x10x1.4	
Lot 3	VQ313618	cut1.3	GQ405266	625W*484QCXX	LQFP 64 10x10x1.4	
Lot 4	9R310042	cut1.1	GQ34321Q	649X*467QCXZ	LQFP 80 12X12X1.4	
Lot 5	9R316240	cut2.3	GQ34529Q	6H5B*469QCXX	LQFP 48 7x7x1.4	
Lot 6	9R322357	cut1.1	GQ409293	665W*455QCXZ	LQFP 64 10x10x1.4	

### 3.2. Test plan and results summary

#### ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	JESD22-A113	24h bake@125°C, 192h/30°C/60%RH 3x Reflow simulation Peak Reflow Temp=260°C	6	308	1848	Lot 1: 0/308 Lot 2: 0/308 Lot 3: 0/308 Lot 4: 0/308 Lot 5: 0/308 Lot 6: Q3'2024	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs <input checked="" type="checkbox"/> After PC	6	77	462	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77 Lot 6: Q3'2024	
TC	JESD22-A104	Ta= -65 to 150°C Cyc= 500 cy <input checked="" type="checkbox"/> After PC	6	77	462	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77 Lot 6: Q3'2024	
THB	JESD22-A101	Ta= 85%HR/85°C/VDD max Duration= 1000hrs <input checked="" type="checkbox"/> After PC	6	77	462	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77 Lot 6: Q3'2024	
UHASt	JESD22-A118	Ta= 130°C/85%RH Duration= 96hrs <input checked="" type="checkbox"/> After PC	6	77	462	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: 0/77 Lot 6: Q3'2024	

#### Electrical Verification Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CDM	JS-002	Voltage= 500V for die 466 500V for die 474 500V for die 484 250V for die 467 500V for die 469 500V for die 455 except pin PC15 250V	6	3	18	Lot 1 : 0/3 Lot 2 : 0/3 Lot 3 : 0/3 Lot 4 : 0/3 Lot 5 : 0/3 Lot 6: Q3'24	

## PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
CA	JESD B100/ B108 ST internal specifications	Construction analysis including POA and BS/PT	6	50	300	Lot 1: 0/50 Lot 2 : 0/50 Lot 3 : 0/50 Lot 4: 0/50 Lot 5: 0/50 Lot 6: Q3'24	NRL202311_0453 NRL202402_0299 NRL202402_0300 NRL202311_0269 NRL202312_0056 Q3'2024

Note: Test method revision reference is the one active at the date of reliability trial execution.

## 4. APPLICABLE AND REFERENCE DOCUMENTS

Remove from below list not applicable documents.

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A101	Temperature Humidity Bias
JESD B100/ B108	Physical dimension

## 5. GLOSSARY

<b>CDM</b>	Electrostatic Discharge - Charged device model
<b>THB</b>	Temperature Humidity Bias
<b>CA</b>	Construction analysis System
<b>HTSL</b>	HTSL Storage Life High temperature storage life
<b>PC</b>	Preconditioning
<b>TC</b>	Temperature Cycling
<b>THB</b>	Temperature Humidity Bias
<b>UHAST</b>	Unbiased HAST (Highly Accelerated Stress Test)
<b>DMS</b>	ST Advanced Documentation Controlled system/ Documentation Management System
<b>BS/PT</b>	Ball Shear/ Pull Test

## 6. REVISION HISTORY

<b>Release</b>	<b>Date</b>	<b>Description</b>
1.0	17/05/2024	Initial Release
2.0	27/06/2024	E40 Crolles qualification results
3.0	05/08/2024	PCN14922 added

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## Public Products List

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**PCN Title :** JSCC (China) LQFP7x7 48L , LQFP10x10 64L and UFQFPN7X7 48L new BOM for STM32H523x and STM32H533x listed product.

**PCN Reference :** MICROCONTROLLERS/24/14922

**Subject :** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32H523CEU6	STM32H523CCT6	STM32H533CET6
STM32H523RET7	STM32H523CET6	STM32H523RET7TR
STM32H533CEU6	STM32H523RCT6	STM32H523CCT7
STM32H523CCU6	STM32H533RET6	STM32H523RCT7TR
STM32H523RCT7	STM32H523RCT6TR	STM32H523RET6

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