

## PRODUCT / PROCESS CHANGE NOTIFICATION

### 1. PCN basic data

1.1 Company	 STMicroelectronics International N.V
1.2 PCN No.	ANALOG MEMS SENSORS/24/14702
1.3 Title of PCN	Additional Front end capacity for HF5CMOS in ST Crolles - Automotive Grade products
1.4 Product Category	See product list
1.5 Issue date	2024-04-18

### 2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.2.2 Marketing Manager	Salvatore DI VINCENZO
2.2.3 Quality Manager	Jean-Marc BUGNARD

### 3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication (SOP 2617)	Front end plant : - Current : UMC Taiwan - New : ST Crolles

### 4. Description of change

	Old	New
4.1 Description	Front end plant : - UMC Taiwan	Front end plant : - UMC Taiwan - ST Crolles
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

### 5. Reason / motivation for change

5.1 Motivation	Progressing on the activities related to HF5CMOS technologies manufacturing double sourcing, ST is glad to announce additional production site in ST Crolles (France) for selected products. This process is already running in ST Crolles since 2014 for similar products.
5.2 Customer Benefit	CAPACITY INCREASE

### 6. Marking of parts / traceability of change

6.1 Description	New Finished good codes
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### 7. Timing / schedule

7.1 Date of qualification results	2024-09-30
7.2 Intended start of delivery	2024-10-15
7.3 Qualification sample available?	Upon Request

### 8. Qualification / Validation

8.1 Description	14702 PCN_Qual_ReportV9XX_UMCtoCrolles (002).pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-04-18

**9. Attachments (additional documentations)**

14702 Public product.pdf  
14702 PCN\_Qual\_ReportV9XX\_UMCtoCrolles (002).pdf

**10. Affected parts**

<b>10. 1 Current</b>		<b>10.2 New (if applicable)</b>
<b>10.1.1 Customer Part No</b>	<b>10.1.2 Supplier Part No</b>	<b>10.1.2 Supplier Part No</b>
	TSV911AIYDT	
	TSV911AIYLT	
	TSV911IYDT	
	TSV911IYLT	
	TSV912AIYDT	
	TSV912AIYST	
	TSV912HYDT	
	TSV912IYDT	
	TSV912IYST	
	TSV914AIYDT	
	TSV914AIYPT	
	TSV914IYDT	
	TSV914IYPT	

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**PRODUCT/PROCESS  
CHANGE NOTIFICATION  
ANALOG MEMS SENSORS/24/14702**

***Analog, Power&discrete, MEMS and Sensor Group***  
**Additional capacity for additional HF5CMOS**



UMC Taiwan



ST Crolles & UMC Taiwan

**WHAT:**

Progressing on the activities related to HF5CMOS technologies manufacturing double sourcing, ST is glad to announce additional production site in ST Crolles (France) for selected products. This process already running in ST Crolles Since 2014 for similar products.

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	
Wafer dimension	8 inches	8 inches	No change
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.

Samples are available, upon request.

**WHY:**

To improve service to ST Customers and increase capacity for the affected technologies.

**HOW:**

HF5CMOS process already qualified in ST Crolles for other products. Extension of the line for additional AMS products is qualified based on qualification plan here attached.

Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

**WHEN:**

Production in ST Crolles for selected products, is forecasted in October 2024.

**Marking and traceability:**

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.

There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

Shipments from new Wafer FAB location will be tracked on the ST Standard Label as showed below:

Manufactured under patents or patents pending

**STMicroelectronics**

Assembled in: 1234567890123456  
Pb-free 2nd Level Interconnect  
MSL: 12 Bag seal date: dd mm yyyy  
PBT: 260 C Category: xx ECOPACK/RoHS

**TYPE: 1234567890123456  
1234567890123456**

Wafer fab code  
will move from  
“LE” to “VJ”

**Total Qty: 12345**

**Trace codes** PPYWWLL1 WX TF  
PPYWWLL2 WX TF

Marking 12345678901234567890

Bulk ID **1234567890123**



Please provide the bulk ID for any inquiry

**Generic ST Standard label**

## Change Qualification Plan

*Double source front end plant qualification  
ST Crolles HCMOS5 and HCMOS 6*

<b>Test vehicle</b>	
<b>Product Lines:</b>	<i>V911, V912, V914, 3021</i>
<b>Product Families:</b>	<ul style="list-style-type: none"><li>Single, dual, and quad rail-to-rail input/output 8 MHz operational amplifiers</li><li>Rail-to-rail 1.8 V high-speed comparator</li></ul>
<b>P/Ns:</b>	<i>TSV911IYLT, TSV912IYST, TSV914IYPT</i>
<b>Product Groups:</b>	<i>AMS</i>
<b>Product Divisions:</b>	<i>General Purpose Analog</i>
<b>Packages:</b>	<i>Sot23-5, MiniSO, TSSOP14</i>
<b>Silicon Process techn.:</b>	<i>HF5CMOS</i>

<b>Locations</b>	
<b>Wafer Diffusion Plants:</b>	<i>ST Crolles 200</i>
<b>EWS Plants:</b>	<i>ST Singapore</i>
<b>Assembly Plants:</b>	<i>Carsem Malaysia, ST Bouskoura (Morocco), TSHT (China), Amkor Philippines</i>
<b>T&amp;F Plants:</b>	<i>Carsem Malaysia, ST Bouskoura (Morocco), TSHT (China) Amkor Philippines</i>

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential qualification risks during the product life using a set of defined test methods.

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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

<b>Document reference</b>	<b>Short description</b>
<b>AEC-Q100</b>	Stress test qualification for automotive grade integrated circuits
<b>AEC-Q006</b>	Guidelines for Characterizing the Electrical Performance of IC Products

## **2 GLOSSARY**

<b>DUT</b>	Device Under Test
<b>PCB</b>	Printed Circuit Board
<b>SS</b>	Sample Size

## **3 QUALIFICATION EVALUATION OVERVIEW**

### **3.1 Objectives**

To Qualify additional products (V9XX) in HF5CMOS in ST Crolles.

### **3.2 Conclusion**

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

## 4 CHANGE CHARACTERISTICS

### 4.1 Change description

Additional source for Selected products in HF5CMOS in ST Crolles

### 4.2 Change details

Material	Current process	additional process	Comment
diffusion location	UMC Taiwan	ST Crolles	
Wafer dimension	8 inches	8 inches	No change
Metallization	AlCu	AlCu	No change
Passivation	PSG/Nitride	PSG/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

### 4.3 Test vehicles description

	P/N TSV911IYLT	P/N TSV912IYDT	P/N TSV912IYST	P/N TSV914IYPT
<b>Wafer/Die fab. information</b>				
Wafer fab manufacturing location	Crolles 200	Crolles 200	Crolles 200	Crolles 200
Technology	HF5CMOS	HF5CMOS	HF5CMOS	HF5CMOS
Process family	HF5CMOS	HF5CMOS	HF5CMOS	HF5CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	850x950 $\mu$ m <sup>2</sup>	1100x1070 $\mu$ m <sup>2</sup>	1100x1070 $\mu$ m <sup>2</sup>	
Bond pad metallization layers	AlCu	AlCu	AlCu	AlCu
Passivation type	PSG + NITRIDE	PSG+Nitride+PIX	PSG + NITRIDE	PSG + NITRIDE
<b>Wafer Testing (EWS) information</b>				
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
<b>Assembly information</b>				
Assembly site	Carsem Malaysia	ST Bouskoura	TSHT	Amkor Ph.
Package description	Sot23-5	SO8	MiniSO8	MiniSO8
Molding compound	Hitachi CEL8240HF	Sumitomo G700KC	Hitachi CEL-9220HF	Sumitomo G700LS
Frame material	Copper	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	QMI519	Epoxy 8601S-25	8200T Henkel	ABLESTICK 8290
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Gold wire 1 mil	Copper wire 1 mil	CuPd wire 1 mi	Gold 0.8mils
Lead finishing process	Preplated frame	Electroplating	Electroplating	Preplated frame
Lead finishing/bump solder material	NiPdAu Pre-plated	Sn	Sn	NiPdAu Pre-plated
<b>Final testing information</b>				
Testing location	Carsem Malaysia	ST Bouskoura	TSHT	Amkor Ph.
				ST Bouskoura

## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicles

Lot #	P/N	Process/ Package	Comments
1	TSV911IYLT	HF5CMOS/Sot23-5	
2	TSV912IYDT	HF5CMOS/SO8	
3	TSV912IYDT	HF5CMOS/SO8	
4	TSV912IYDT	HF5CMOS/SO8	
5	TSV912IYST	HF5CMOS/MiniSO8	TSHT
6	TSV912IYST	HF5CMOS/MiniSO8	Amkor Ph
7	TSV914IYPT	HF5CMOS/TSSOP14	

### 5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS							Note
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	
<b>Die Oriented Tests</b>													
<b>HTB</b> High Temp. Bias	N	JESD22 A-108	T <sub>j</sub> = 125°C, BIAS	77	168H 500H 1000H 2000H	0/77 w14 w22	w22 w26 w34	w22 w26 w34	w22 w26 w34	0/77 0/77 w20	0/77 0/77 0/77	0/77 0/77 0/77	150°C for TV2,3,4
<b>HTSL</b> High Temp. Storage Life	N	JESD22 A-103	T <sub>a</sub> = 150°C	77	500H 1000 H 2000H	0/77 0/77 w23	w20 w24 w32	w18 w22 w30	w18 w22 w30	0/77 0/77 w14	0/77 0/77 w21	0/77 0/77 W15	175°C for TV2,3,4
<b>ELFR</b> Early Life Failure Rate	N	AEC Q100 - 008	T <sub>a</sub> =125°C	800	48H	0/800	w20	w20	w20	0/800	0/800	0/800	
<b>Package oriented test</b>													
<b>PC</b> Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ T <sub>a</sub> =85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	PASS	w19	w17	w17	PASS	PASS	PASS	
<b>UHAST</b> Unbiased humidity accelerated stress	Y	JESD22 A-102	P <sub>a</sub> =2Atm / T <sub>a</sub> =121°C	77	96 H	w17	w20	w18	w18	0/77	0/77	0/77	
<b>TC</b> Temperature Cycling	Y	JESD22 A-104	T <sub>a</sub> = -65°C to 150°C	77	500cy 1000cy 2000cy 3500cy	w19 w25 w34 w30	w21 w26 w35 w44	w21 w26 w35 w44	w21 w26 w35 w44	0/77 0/77 w14	0/77 0/77 w23	0/77 0/77 w15	
<b>THB</b> Temperature Humidity Bias	Y	JESD22 A-101	T <sub>a</sub> = 85°C, RH = 85%, BIAS	77	168H 500 H 1000 H 2000H	0/77 0/77 w16	w22 w26 w34	w22 w26 w34	w22 w26 w34	0/77 0/77 w20	0/77 0/77 0/77	0/77 0/77 0/77	
<b>Other Tests</b>													
<b>ESD</b> Electro Static Discharge	-	AEC Q101- 001, 002 and 005	HBM	3		0/3	w20			0/3	0/3	0/3	
			CDM	3		0/3	w20			0/3	0/3	0/3	
<b>LU</b> Latch up	N	AEC Q100-004	LU	6		0/6	w20			0/6	0/6	0/6	

## 5.3 Electrical distribution comparison

### V911 – EWS

Test Name	units	Mean		Comment	
		UMC	Crolles		
P106_*8 , lcc	uA	766.312	688.222	78.09	Cpk > 1,67
P101_A8 , Vio	uV	-600.494	-427.98	-172.514	Cpk > 1,67
P106_*9 , lcc	uA	760.924	680.085	80.839	Cpk > 1,67
P101_A9 , Vio	uV	-29.4062	225.56	-254.966	Cpk > 1,67
P117_A2 , Voh	V	2.49086	2.48481	0.00605	Not a Gaussian Distribution
P117_A2 , Vol	mV	8.47935	11.1464	-2.66705	Not a Gaussian Distribution
P101_A2 , Vio	uV	-602.251	-471.729	-130.522	Not a Gaussian Distribution
P106_*1 , lcc	uA	831.23	748.965	82.265	Cpk > 1,67
P109_A1 , cmr	dB	76.1482	86.8422	-10.694	Not a Gaussian Distribution
P105_A1, SVR	dB	86.659	119.086	-32.427	Not a Gaussian Distribution
P102_A1 , lio	pA	7.19896	-38.4946	45.6935	Cpk > 1,67
P103_A1 , libn	pA	8.72208	8.33297	0.38911	Cpk > 1,67
P103_A1 , libp	pA	1.52311	46.8276	-45.3045	Cpk > 1,67
P117_A1 , Voh	V	2.45252	2.44459	0.00793	Cpk > 1,67
P117_A1 , Vol	mV	32.2173	35.3584	-3.1411	Cpk > 1,67
P117_A4 , Voh	V	4.98943	4.98145	0.00798	Cpk > 1,67
P117_A4 , Vol	mV	11.7585	12.4552	-0.6967	Cpk > 1,67
P113_A1 , SRn	V/uS	4.82548	4.40797	0.41751	Not a Gaussian Distribution
P113_A1 , SRp	V/uS	4.20608	3.54564	0.66044	Not a Gaussian Distribution
P113_A2 , SRn	V/uS	4.8063	5.09323	-0.28693	Not a Gaussian Distribution
P113_A2 , SRp	V/uS	4.58286	3.63412	0.94874	Not a Gaussian Distribution
P151_A1 , llnp input-	nA	2.55934	0.234381	2.32496	Cpk > 1,67
P151_A1 , llpp input+	nA	1.53404	0.26727	1.26677	Cpk > 1,67
P151_A1 , llnn input-	nA	2.39735	0.193671	2.20368	Cpk > 1,67
P151_A1 , llpn input+	nA	1.41608	0.248779	1.16730	Cpk > 1,67

## V912 EWS

Test Name	units	Mean		UMC-Crolles	Comment
		UMC	CROLLES		
P106_*9 , lcc	uA	725.088	722.931	2.157	Cpk > 1,67
P101_A9 , Vio	uV	30.8077	-181.997	212.8047	Cpk > 1,67
P101_B9 , Vio	uV	-14.840	-285.188	270.3476	Cpk > 1,67
P117_A0 , Voh	V	2.48608	2.48409	0.00199	Not a Gaussian Distribution
P117_B0 , Voh	V	2.48653	2.48473	0.0018	Not a Gaussian Distribution
P117_A0 , Vol	mV	15.5041	17.2684	-1.7643	Not a Gaussian Distribution
P117_B0 , Vol	mV	15.2299	17.174	-1.9441	Not a Gaussian Distribution
P101_A2 , Vio	uV	-585.46	-745.22	159.755	Not a Gaussian Distribution
P101_B2 , Vio	uV	-614.03	-875.291	261.26	Not a Gaussian Distribution
P106_*1 , lcc	uA	792.611	797.47	-4.859	Cpk > 1,67
P104_A3 , Avd	V/mV	32.9624	35.5728	-2.6104	Not a Gaussian Distribution
P104_B3 , Avd	V/mV	34.7262	35.5808	-0.8546	Not a Gaussian Distribution
P105_A1 , SVR	dB	86.3098	87.2272	-0.9174	Not a Gaussian Distribution
P105_B1 , SVR	dB	86.1206	86.5096	-0.389	Not a Gaussian Distribution
P102_A1, lio	pA	4.45932	7.85585	-3.39653	Cpk > 1,67
P102_B1, lio	pA	1.55138	7.30174	-5.75036	Cpk > 1,67
P103_A1, libn	pA	7.72733	12.6986	-4.97127	Cpk > 1,67
P103_B1, libn	pA	4.69471	9.37855	-4.68384	Cpk > 1,67
P103_A1, libp	pA	3.26801	4.84275	-1.57474	Cpk > 1,67
P103_B1, libp	pA	3.14334	2.0768	1.06654	Cpk > 1,67
P117_A1 , Voh	V	2.44775	2.44701	0.00074	Not a Gaussian Distribution
P117_B1 , Voh	V	2.44997	2.44966	0.00031	Not a Gaussian Distribution
P117_A1 , Vol	mV	41.8839	41.9784	-0.0945	Not a Gaussian Distribution
P117_B1 , Vol	mV	42.1126	42.0317	0.0809	Not a Gaussian Distribution
P113_A2 , SRn	V/uS	4.53224	4.62231	-0.09007	Not a Gaussian Distribution
P113_B2 , SRn	V/uS	4.49724	4.57643	-0.07919	Not a Gaussian Distribution
P113_A2 , SRp	V/uS	3.57112	3.55587	0.01525	Not a Gaussian Distribution
P113_B2 , SRp	V/uS	3.57303	3.57424	-0.00121	Not a Gaussian Distribution

## V914 EWS

Test Name	units	mean		UMC-CROLLES	Comment
		UMC	CROLLES		
P106_*8 , lcc	uA	763.03	790.415	-27.385	Cpk > 1,67
P101_A8 , Vio	uV	-536.12	-411.07	-124.813	Cpk > 1,67
P101_B8 , Vio	uV	-385.50	-669.51	284.005	Cpk > 1,67
P101_C8 , Vio	uV	-446.49	-647.19	200.696	Cpk > 1,67
P101_D8 , Vio	uV	-440.09	-434.88	-5.208	Cpk > 1,67
P106 *9 , lcc	uA	755.649	757.445	-1.796	Cpk > 1,67
P101_A9 , Vio	uV	75.1539	49.0956	26.0583	Cpk > 1,67
P101_B9 , Vio	uV	141.341	-191.11	332.452	Cpk > 1,67
P101_C9 , Vio	uV	141.14	-319.66	460.807	Cpk > 1,67
P101_D9 , Vio	uV	119.884	-121.09	240.975	Cpk > 1,67
P117_A2 , Voh	V	2.48024	2.47781	0.00243	Not a Gaussian Distribution
P117_B2 , Voh	V	2.48009	2.4778	0.00229	Not a Gaussian Distribution
P117_C2 , Voh	V	2.48015	2.47809	0.00206	Not a Gaussian Distribution
P117_D2 , Voh	V	2.48007	2.47765	0.00242	Not a Gaussian Distribution
P117_A2 , Vol	mV	19.7001	21.7368	-2.0367	Not a Gaussian Distribution
P117_B2 , Vol	mV	19.4585	21.7162	-2.2577	Not a Gaussian Distribution
P117_C2 , Vol	mV	19.2676	21.5811	-2.3135	Not a Gaussian Distribution
P117_D2 , Vol	mV	19.3944	21.5966	-2.2022	Not a Gaussian Distribution
P106 *1 , lcc	uA	824.792	843.932	-19.14	Not a Gaussian Distribution
P101_A1 , Vio	uV	-402.70	-316.01	-86.693	Cpk > 1,67
P101_B1 , Vio	uV	-258.83	-564.52	305.69	Cpk > 1,67
P101_C1 , Vio	uV	-319.68	-542.40	222.72	Cpk > 1,67
P101_D1 , Vio	uV	-313.81	-330.98	17.169	Cpk > 1,67
P104_A1 , Avd	V/mV	140.508	94.3814	46.1266	Not a Gaussian Distribution
P104_B1 , Avd	V/mV	23.9459	30.2155	-6.2696	Not a Gaussian Distribution
P104_C1 , Avd	V/mV	822.217	844.967	-22.75	Not a Gaussian Distribution
P104_D1 , Avd	V/mV	43.2953	29.9861	13.3092	Not a Gaussian Distribution
P104_A3 , Avd	V/mV	348.742	216.893	131.849	Not a Gaussian Distribution
P104_B3 , Avd	V/mV	39.9565	46.6902	-6.7337	Not a Gaussian Distribution
P104_C3 , Avd	KV/mV	1.24384	1.30622	-0.06238	Not a Gaussian Distribution
P104_D3 , Avd	V/mV	90.3284	45.733	44.5954	Not a Gaussian Distribution
P109_A1 , cmr	dB	75.4013	77.5558	-2.1545	Not a Gaussian Distribution
P109_B1 , cmr	dB	76.5961	76.9551	-0.359	Not a Gaussian Distribution
P109_C1 , cmr	dB	75.606	79.2174	-3.6114	Not a Gaussian Distribution
P109_D1 , cmr	dB	75.9547	79.5598	-3.6051	Not a Gaussian Distribution
P109_A2 , cmr	dB	82.2232	84.2806	-2.0574	Not a Gaussian Distribution
P109_B2 , cmr	dB	83.1786	84.032	-0.8534	Not a Gaussian Distribution
P109_C2 , cmr	dB	82.3953	85.8578	-3.4625	Not a Gaussian Distribution
P109_D2 , cmr	dB	82.5781	86.1079	-3.5298	Not a Gaussian Distribution
P105_A1 , SVR	dB	90.6595	91.2341	-0.5746	Not a Gaussian Distribution
P105_B1 , SVR	dB	87.8518	87.7537	0.0981	Not a Gaussian Distribution
P105_C1 , SVR	dB	109.981	105.529	4.452	Not a Gaussian Distribution
P105_D1 , SVR	dB	87.9583	88.7096	-0.7513	Not a Gaussian Distribution
P102_A1 , lio	pA	2.10357	26.7891	-24.6855	Cpk > 1,67
P102_B1 , lio	pA	5.72225	0.436002	5.286	Cpk > 1,67
P102_C1 , lio	pA	0.686095	3.02762	-2.341525	Cpk > 1,67
P102_D1 , lio	pA	-0.79474	0.544993	-1.33974	Cpk > 1,67
P103_A1 , libn	pA	5.12771	31.0372	-25.9095	Cpk > 1,67
P103_B1 , libn	pA	6.23407	4.81894	1.41513	Cpk > 1,67
P103_C1 , libn	pA	4.53991	9.812	-5.27209	Cpk > 1,67
P103_D1 , libn	pA	3.58248	7.48702	-3.90454	Cpk > 1,67
P103_A1 , libp	pA	3.02414	4.24815	-1.22401	Cpk > 1,67
P103_B1 , libp	pA	0.51182	4.38294	-3.871	Cpk > 1,67
P103_C1 , libp	pA	3.85381	6.78438	-2.93057	Cpk > 1,67

P103_D1	, libp	pA	4.37722	6.94203	-2.56481	Cpk > 1,67
P121_A1	, GBP	MHz	7.11254	7.4432	-0.33066	Cpk > 1,67
P121_B1	, GBP	MHz	7.13173	7.43207	-0.30034	Cpk > 1,67
P121_C1	, GBP	MHz	7.16666	7.44103	-0.27437	Cpk > 1,67
P121_D1	, GBP	MHz	7.02064	7.43227	-0.41163	Cpk > 1,67
P117_A1	, Voh	V	2.43804	2.43587	0.00217	Cpk > 1,67
P117_B1	, Voh	V	2.43775	2.43583	0.00192	Cpk > 1,67
P117_C1	, Voh	V	2.43806	2.43688	0.00118	Cpk > 1,67
P117_D1	, Voh	V	2.43755	2.43644	0.00111	Cpk > 1,67
P117_A1	, Vol	mV	47.9332	48.0937	-0.1605	Cpk > 1,67
P117_B1	, Vol	mV	47.8121	48.0752	-0.2631	Cpk > 1,67
P117_C1	, Vol	mV	46.9807	46.7881	0.1926	Cpk > 1,67
P117_D1	, Vol	mV	47.5968	46.8972	0.6996	Cpk > 1,67
P117_A4	, Voh	V	4.9782	4.97555	0.00265	Cpk > 1,67
P117_B4	, Voh	V	4.97753	4.9749	0.00263	Cpk > 1,67
P117_C4	, Voh	V	4.97767	4.9757	0.00197	Cpk > 1,67
P117_D4	, Voh	V	4.9777	4.97495	0.00275	Cpk > 1,67
P117_A4	, Vol	mV	22.5611	24.1425	-1.5814	Cpk > 1,67
P117_B4	, Vol	mV	21.9439	23.8952	-1.9513	Cpk > 1,67
P117_C4	, Vol	mV	21.643	24.0795	-2.4365	Cpk > 1,67
P117_D4	, Vol	mV	21.9313	23.6911	-1.7598	Cpk > 1,67
P117_A3	, Voh	V	4.89438	4.89209	0.00229	Cpk > 1,67
P117_B3	, Voh	V	4.8933	4.89141	0.00189	Cpk > 1,67
P117_C3	, Voh	V	4.89394	4.89368	0.00026	Cpk > 1,67
P117_D3	, Voh	V	4.89306	4.89283	0.00023	Cpk > 1,67
P117_A3	, Vol	mV	79.1761	77.041	2.1351	Cpk > 1,67
P117_B3	, Vol	mV	78.9088	76.7588	2.15	Cpk > 1,67
P117_C3	, Vol	mV	77.3601	74.6304	2.7297	Cpk > 1,67
P117_D3	, Vol	mV	78.5987	74.3835	4.2152	Cpk > 1,67
P137_A1	, Isk	mA	29.421	37.8107	-8.3897	Cpk > 1,67
P137_B1	, Isk	mA	29.3704	37.7739	-8.4035	Cpk > 1,67
P137_C1	, Isk	mA	29.3991	38.2373	-8.8382	Cpk > 1,67
P137_D1	, Isk	mA	29.39	38.1766	-8.7866	Cpk > 1,67
P137_A1	, Isr	mA	-32.364	-41.094	8.7295	Cpk > 1,67
P137_B1	, Isr	mA	-32.419	-41.083	8.6634	Cpk > 1,67
P137_C1	, Isr	mA	-32.422	-41.215	8.7932	Cpk > 1,67
P137_D1	, Isr	mA	-32.386	-41.256	8.8699	Cpk > 1,67
P113_A1	, SRn	V/uS	3.86922	4.98936	-1.12014	Cpk > 1,67
P113_B1	, SRn	V/uS	3.88008	5.05052	-1.17044	Cpk > 1,67
P113_C1	, SRn	V/uS	3.86763	5.00786	-1.14023	Cpk > 1,67
P113_D1	, SRn	V/uS	3.89941	4.96347	-1.06406	Cpk > 1,67
P113_A1	, SRp	V/uS	3.10274	4.18262	-1.07988	Cpk > 1,67
P113_B1	, SRp	V/uS	3.10161	4.23478	-1.13317	Not a Gaussian Distribution
P113_C1	, SRp	V/uS	3.10982	4.20542	-1.0956	Not a Gaussian Distribution
P113_D1	, SRp	V/uS	3.11058	4.18006	-1.06948	Not a Gaussian Distribution
P113_A2	, SRn	V/uS	4.4428	4.94268	-0.49988	Not a Gaussian Distribution
P113_B2	, SRn	V/uS	4.45336	4.98139	-0.52803	Not a Gaussian Distribution
P113_C2	, SRn	V/uS	4.40797	4.92825	-0.52028	Not a Gaussian Distribution
P113_D2	, SRn	V/uS	4.45672	4.93795	-0.48123	Not a Gaussian Distribution
P113_A2	, SRp	V/uS	3.39771	4.1404	-0.74269	Not a Gaussian Distribution
P113_B2	, SRp	V/uS	3.41876	4.18408	-0.76532	Not a Gaussian Distribution
P113_C2	, SRp	V/uS	3.42829	4.17946	-0.75117	Not a Gaussian Distribution
P113_D2	, SRp	V/uS	3.42465	4.14815	-0.7235	Not a Gaussian Distribution

## Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTOL</b> High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
<b>HTB</b> High Temperature Bias		
<b>HTRB</b> High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.
<b>HTFB / HTGB</b> High Temperature Forward (Gate) Bias	<ul style="list-style-type: none"> <li>• low power dissipation;</li> <li>• max. supply voltage compatible with diffusion process and internal circuitry limitations;</li> </ul>	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>ELFR</b> Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	<p>As stand-alone test: to investigate the moisture sensitivity level.</p> <p>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.</p> <p>The typical failure modes are "pop corn" effect and delamination.</p>
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
<b>THS</b> Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
<b>PTC</b> Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not induced by fixture or handling.
<b>EV</b> External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,...).
<b>LI</b> Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for re-assembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
<b>WBP</b> Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
<b>WBS</b> Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
<b>DS</b> Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
<b>PD</b> Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
<b>SD</b> Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
<b>Other</b>		
<b>ESD</b> Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. <b>CBM:</b> Charged Device Model <b>HBM:</b> Human Body Model <b>MM:</b> Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
<b>LU</b> Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

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**PCN Title :** Additional Front end capacity for HF5CMOS in ST Crolles - Automotive Grade products

**PCN Reference :** ANALOG MEMS SENSORS/24/14702

**Subject :** Public Products List

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TSL6202IYST	TSV912AIYDT	TSV912AIYST
TSV914IYPT	TSL6201IYLT	TSV911AIYDT
TSV911IYDT	TSV914IYDT	TSV912HYDT
TSV914AIYPT	TSV911IYLT	TSV914AIYDT

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