PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-APD/12/7571
Dated 03 Dec 2012

Wafer dimension change from 5’’ to 6’’ for CMOS metal gate technology in ST Singapore

Table 1. Change Implementation Schedule

Forecasted implementation date for change	31-Jan-2013
Forecasted availability date of samples for customer	30-Nov-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	26-Nov-2012
Estimated date of changed product first shipment	04-Mar-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Product marking change
Reason for change	To rationalize wafer manufacturing processes.
Description of the change	Progressing on the activities related to CMOS metal gate manufacturing processes, ST is glad to announce availability of 6 inches wafer production line, for Standard & HiRel products of Analog Mems & Sensors group. Please note that samples of test vehicles are available upon request and other samples from mid-January upon request. You can enter a non-standard samples order in the system with in comment "PCN#7571 qualification". Then send the SO# to Angelique DUCHENE for samples availability management.
Change Product Identification	Date code & lot number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt **PCN AMS-APD/12/7571**

Please sign and return to STMicroelectronics Sales Office **Dated 03 Dec 2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

....

....

....

....

....

....

....

....

DOCUMENT APPROVAL

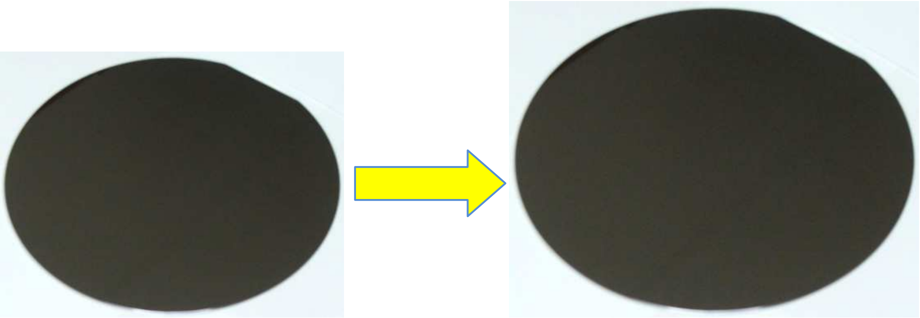
Name	Function
Grillo, Lionel	Marketing Manager
De marco, Alberto	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS-APD/12/7571

Analog, MEMS and Sensor Group

Wafer dimension change from 5 inches to 6 inches for CMOS metal gate technology in ST Singapore



5 inches 6 inches

CMOS metal gate

WHAT:

Progressing on the activities related to CMOS metal gate manufacturing processes, ST is glad to announce availability of 6 inches wafer production line, for AMS products.

Material	Current process 5 inches CMOS MG	Modified process 6 inches CMOS MG	Comment
diffusion location	ST Ang Mo Kio (Singapore) ST AMJ9	ST Ang Mo Kio (Singapore) ST AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical character recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox	Pvapox	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.
Samples of test vehicles are available upon request and other samples from mid-January upon request.

WHY:
To upgrade manufacturing line from 5 inches to 6 inches in order to improve customer service.

HOW:
The change that covers AMS (Analog, Mems & Sensors) products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in ST Singapore in 6 inches for AMS is forecasted in January 2013 for CMOS metal gate technology.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Change Qualification Plan

CMOS metal gate transfer 5 to 6 inches

Test vehicle	
Product Lines:	*P51B, P541, P10B*
Product Families:	*Logic*
P/Ns:	*HCF4051YM013TR,* *HCF4541M013TR* *HCF4010YM013TR*
Product Groups:	*AMS*
Product Divisions:	*Analog*
Product BUs:	*Hirel&standard products.*
Packages:	*SO14/SO16*
Silicon Process techn.:	*CMOS metal gate*

Locations	
Wafer Diffusion Plants:	*ST Singapore*
EWS Plants:	*ST Singapore*
Assembly Plants:	*ST Bouskoura*
T&F Plants:	*ST Bouskoura*
Reliability Lab.:	*ST Catania*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	08-Nov-2012	16	JM Bugnard	First issue

Reference document :
REL-6043-304W-12

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	09 November-2012	8	Angelo Basile	Giovanni Presti	Intermediate Report

REL-6043-332W-12

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	09 Nov -2012	8	Angelo Basile	Giovanni Presti	Preliminary Report

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential qualification risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
AEC-Q001	Guidelines for part average testing
AEC-Q003	Guidelines for Characterizing the Electrical Performance of IC Products
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

Through this qualification plan, the CMOS metal gate technology transfer is evaluated, to be diffused at ST Singapore in 6 inches instead of 5 inches.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

Transfer of CMOS metal gate technology from 5 inches to 6 inches

4.2 Change details

Material	Current process 5 inches CMOS MG	Modified process 6 inches CMOS MG	Comment
diffusion location	ST Ang Mo Kio (Singapore) AMJ9	ST Ang Mo Kio (Singapore) AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical character recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox	Pvapox	No change
EWS	ST Singapore	ST Singapore	No change

4.3 Test vehicles description

	P/N HCF4051YM013TR	P/N HCF4541M013TR	P/N HCF4010YM013TR
Wafer/Die fab. information			
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore
Technology	CMOS Metal gate	CMOS Metal gate	CMOS Metal gate
Process family	CMOSMG	CMOSMG	CMOSMG
Die finishing back side	Lapped silicon	Lapped silicon	Lapped silicon
Die size	1480x1780	1608 *1764	1294x1088
Bond pad metallization layers	AlSi	AlSi	AlSi
Passivation type	Pvapox	Pvapox	Pvapox
Wafer Testing (EWS) information			
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1000	CTS600	ASL1000
Test program	TP51BYW 2	C4541E2 00	TP10BYW 1
Assembly information			
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO16	SO14	SO16
Molding compound	Sumitomo G700K	Sumitomo G630AY	Sumitomo G700K
Frame material	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	Abklestick 8601-S25	Abklestick 8601-S25	Abklestick 8601-S25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Copper 1 mil	Copper 1 mil	Copper 1 mil
Lead finishing process	Preplated frame	Electroplating	Preplated frame
Lead finishing/bump solder material	NiPdAgAu	Sn	NiPdAgAu
Final testing information			
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Product Line	Comments
1	HCF4051YM013TR	CMOSMG/SO16	P51B	
2	HCF4541M013TR	CMOSMG/SO14	P541	
3	HCF4010YM013TR	CMOSMG/SO16	P10B	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125℃, BIAS	77	168H 500H	0/77 0/77	0/77	(1)	
HTSL High Temp. Storage Life	N	JESD22 A-103	Ta = 150℃	45	168H 500 H	0/45 0/45		(1)	
ELFR Early Life Failure Rate	N	AEC Q100 - 008		1600	48H	0/800	0/800	(1)	
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times	231	Final	PASS		(1)	
AC Auto Clave (Pressure Pot)	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	77	168 H	0/77		(1)	
TC Temperature Cycling	Y	JESD22 A-104	Ta = -65℃ to 150℃	77	100cy 200cy	0/77 0/77		(1)	
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS	77	168H 500 H	0/77 0/77		(1)	
Other Tests									
ESD Electro Static Discharge	-	AEC Q101-001, 002 and 005	HBM		1KV	3 (2kV)	3	(1)	
			CDM		750V	3	3	(1)	
			MM		150V	3 (200V)	3	(1)	

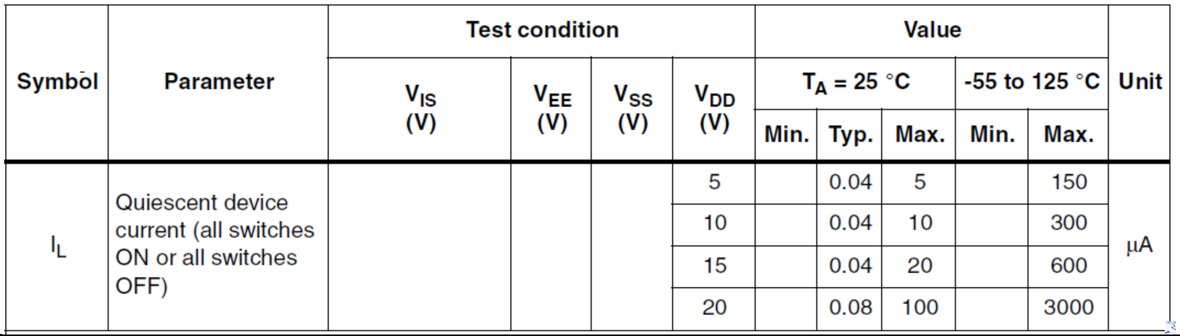
(1) Electrical characterization only

6 ANNEXES

6.1 Comparison Data Results

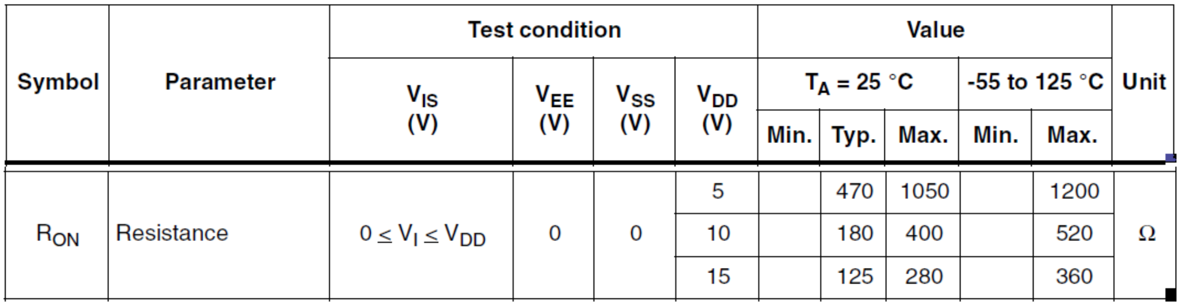
6.1.1 Electrical Data

Test vehicle 1: HCF4051YM013TR



Symbol	Parameter	Test condition				Value					Unit
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_A = 25 °C			-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent device current (all switches ON or all switches OFF)				5		0.04	5		150	µA
					10		0.04	10		300	
					15		0.04	20		600	
					20		0.08	100		3000	

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
IL (Quiescent Device current) @ Vdd=10V	uA	0.12	>2	0.08	>2	Conform
IL (Quiescent Device current) @ Vdd=10V	uA	0.02	>2	0.02	>2	Conform
IL (Quiescent Device current) @ Vdd=10V	uA	0.03	>2	0.03	>2	Conform
IL (Quiescent Device current) @ Vdd=10V	uA	0.02	>2	0.02	>2	Conform
IL (Quiescent Device current) @ Vdd=20V	uA	0.38	>2	0.71	>2	Conform
IL (Quiescent Device current) @ Vdd=20V	uA	0.02	>2	0.00	>2	Conform
IL (Quiescent Device current) @ Vdd=20V	uA	0.04	>2	0.01	>2	Conform
IL (Quiescent Device current) @ Vdd=20V	uA	0.03	>2	0.00	>2	Conform



Symbol	Parameter	Test condition				Value					Unit
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_A = 25 °C			-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	
R_{ON}	Resistance	$0 \leq V_I \leq V_{DD}$	0	0	5		470	1050		1200	Ω
					10		180	400		520	
					15		125	280		360	

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
RON Vcc GND 5V	OHM	254.84	>2	235.96	>2	Conform
RON Vcc GND 10V	OHM	159.65	>2	150.49	>2	Conform
RON Vcc GND 15V	OHM	122.51	>2	113.58	>2	Conform

Symbol	Parameter	Test condition				Value					Unit
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_A = 25 °C			-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	
I_{IH}, I_{IL}	Input leakage current	V_I = 0/18 V			18		$\pm 10^{-3}$	±0.1		±1	µA

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
ILH_Inp A	nA	-17.66	>2	-8.35	>2	Conform
ILH_Inp B	nA	4.91	>2	3.08	>2	Conform
ILH_Inp_C	nA	1.14	>2	-0.10	>2	Conform
ILH_Inp INH	nA	7.94	>2	5.33	>2	Conform
ILL_Inp A	nA	-4.15	>2	-1.98	>2	Conform
ILL_Inp_B	nA	-5.13	>2	-5.44	>2	Conform
ILL_Inp_C	nA	-6.30	>2	-5.52	>2	Conform
ILL_Inp_INH	nA	-24.58	>2	-15.42	>2	Conform

Symbol	Parameter	Test condition				Value					Unit
		V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_A = 25 °C			-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	
OFF(1)	Channel leakage current (any channel OFF)		0	0	18		±0.1	100		1000	nA

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
IOFF3_pin13	nA	8.04	>2	6.42	>2	Conform
IOFF3_pin14	nA	7.08	>2	3.57	>2	Conform
IOFF3_pin15	nA	-14.80	>2	-12.90	>2	Conform
IOFF3_pin12	nA	-8.02	>2	-6.42	>2	Conform
IOFF3_pin1	nA	-22.60	>2	-19.99	>2	Conform
IOFF3_pin5	nA	16.08	>2	12.65	>2	Conform
IOFF3_pin2	nA	14.06	>2	7.22	>2	Conform
IOFF3_pin4	nA	-15.27	>2	-11.03	>2	Conform
IOFF7_pin3	nA	-59.65	>2	-43.51	>2	Conform
IOFF6_pin13	nA	-5.48	>2	-4.41	>2	Conform
IOFF6_pin14	nA	3.73	>2	3.58	>2	Conform
IOFF6_pin15	nA	-5.69	>2	-4.54	>2	Conform
IOFF6_pin12	nA	3.29	>2	2.80	>2	Conform
IOFF6_pin1	nA	-2.91	>2	-1.08	>2	Conform
IOFF6_pin5	nA	-5.35	>2	-4.15	>2	Conform
IOFF6_pin2	nA	4.43	>2	3.93	>2	Conform
IOFF6_pin4	nA	3.96	>2	3.49	>2	Conform
IOFF10_pin3	nA	9.99	>2	11.05	>2	Conform

Test vehicle 2 : HCF4541M013TR

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
I_I	Input Leakage Current	0/18	Any Input		18		$\pm10^{-5}$	±0.1		±1		±1	µA

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
A INPUTS L LEAK	nA	32.34	>2	6.46	>2	Conform
A INPUTS H LEAK	nA	13.77	>2	2.25	>2	Conform

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.55	-3.1		-1.08		-1.08		mA
		0/5	4.6	<1	5	-5	-10		-3		-4.1		
		0/10	9.5	<1	10	-4	-8		-3.3		-3.3		
		0/15	13.5	<1	15	-10	-20		-8.4		-8.4		

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
IOH (ouput drive current)	mA	-6.20	>2	-5.25	>2	Conform

Test vehicle 3 : HCF4010YM013TR

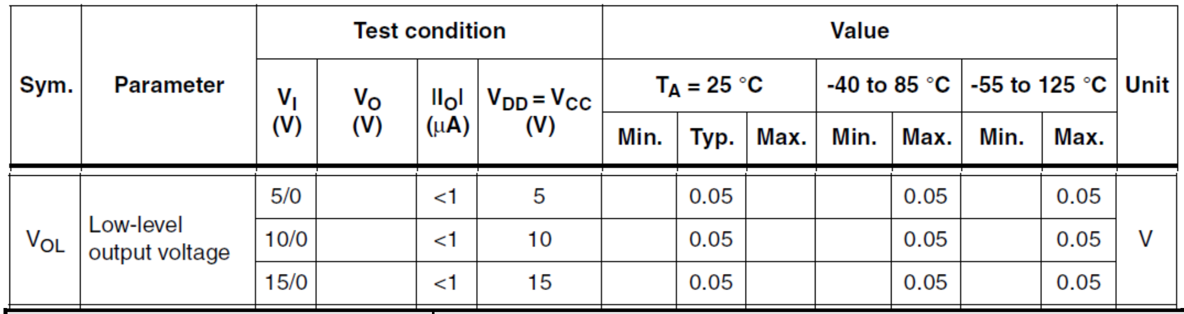
Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	$V_{DD} = V_{CC}$ (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent current	0/5			5		0.02	1		30		30	µA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
Idd Pattern 1 (15V)	µA	0.3	>2	0.02	>2	Conform
Idd Pattern 2 (15V)	µA	0.2	>2	0.01	>2	Conform
Idd Pattern 3 (15V)	µA	0.2	>2	0.05	>2	Conform
Idd Pattern 4 (15V)	µA	0.1	>2	0.09	>2	Conform
Idd Pattern 1 (20V)	µA	0.2	>2	0.03	>2	Conform
Idd Pattern 2 (20V)	µA	0.2	>2	0.02	>2	Conform
Idd Pattern 3 (20V)	µA	0.2	>2	0.08	>2	Conform
Idd Pattern 4	µA	0.1	>2	0.12	>2	Conform

Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	$V_{DD} = V_{CC}$ (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	High-level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
VOH PIN 2 (5V)	V	5.00	>2	4.99	>2	Conform
VOH PIN 4 (5V)	V	5.00	>2	4.99	>2	Conform
VOH PIN 6 (5V)	V	5.00	>2	5.00	>2	Conform
VOH PIN 10 (5V)	V	5.00	>2	5.01	>2	Conform
VOH PIN 12 (5V)	V	5.00	>2	5.01	>2	Conform
VOH PIN 15 (5V)	V	5.00	>2	5.00	>2	Conform
VOH PIN 2 (10V)	V	10.00	>2	10.00	>2	Conform
VOH PIN 4 (10V)	V	10.00	>2	10.00	>2	Conform
VOH PIN 6 (10V)	V	10.00	>2	10.00	>2	Conform
VOH PIN 10 (10V)	V	10.00	>2	10.09	>2	Conform
VOH PIN 12 (10V)	V	10.00	>2	10.07	>2	Conform

VOH PIN 15 (10V)	V	10.00	>2	10.05	>2	Conform
VOH PIN 2 (15V)	V	15.00	>2	15.00	>2	Conform
VOH PIN 4 (15V)	V	15.00	>2	15.00	>2	Conform
VOH PIN 6 (15V)	V	15.00	>2	15.01	>2	Conform
VOH PIN 10 (15V)	V	14.99	>2	15.09	>2	Conform
VOH PIN 12 (15V)	V	15.00	>2	15.12	>2	Conform
VOH PIN 15 (15V)	V	14.99	>2	15.02	>2	Conform



Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	$V_{DD} = V_{CC}$ (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low-level output voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	

Parameter		Results				
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	
VOL PIN 2 (5V)	mV	8.68	>2	10.20	>2	Conform
VOL PIN 4 (5V)	mV	7.40	>2	8.92	>2	Conform
VOL PIN 6 (5V)	mV	6.68	>2	7.96	>2	Conform
VOL PIN 10 (5V)	mV	6.10	>2	5.00	>2	Conform
VOL PIN 12 (5V)	mV	6.98	>2	5.72	>2	Conform
VOL PIN 15 (5V)	mV	7.75	>2	7.36	>2	Conform
VOL PIN 2 (10V)	mV	5.94	>2	7.18	>2	Conform
VOL PIN 4 (10V)	mV	4.14	>2	5.13	>2	Conform
VOL PIN 6 (10V)	mV	3.37	>2	4.25	>2	Conform
VOL PIN 10 (10V)	mV	3.13	>2	2.11	>2	Conform
VOL PIN 12 (10V)	mV	3.73	>2	2.83	>2	Conform
VOL PIN 15 (10V)	mV	4.48	>2	4.25	>2	Conform
VOH PIN 15 (10V)	V	14.99	>2	15.02	>2	Conform
VOL PIN 2 (15V)	mV	4.59	>2	5.75	>2	Conform
VOL PIN 4 (15V)	mV	2.48	>2	3.70	>2	Conform
VOL PIN 6 (15V)	mV	1.94	>2	2.59	>2	Conform
VOL PIN 10 (15V)	mV	1.16	>2	1.98	>2	Conform
VOL PIN 12 (15V)	mV	1.74	>2	2.19	>2	Conform
VOL PIN 15 (15V)	mV	2.81	>2	4.07	>2	Conform

Conclusion: New version in line with requirements.

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

ⓒ2012 STMicroelectronics - All rights reserved.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morroco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Public Products List

PCN Title : Wafer dimension change from 5’’ to 6’’ for CMOS metal gate technology in ST Singapore
PCN Reference : AMS-APD/12/7571
PCN Created on : 27-NOV-2012

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

HCF4001BEY
HCF4001M013TR
HCF4007UBEY
HCF4007UBM013TR
HCF40103BEY
HCF40106BEY
HCF40106M013TR
HCF4010M013TR
HCF4011BEY
HCF4011M013TR
HCF4013BEY
HCF4013M013TR
HCF4014BEY
HCF4014M013TR
HCF4016BEY
HCF4017BEY
HCF4017M013TR
HCF4019M013TR
HCF4020BEY
HCF4020M013TR
HCF4021BEY
HCF4021M013TR
HCF4024BEY
HCF4024M013TR
HCF4025BEY
HCF4025M013TR
HCF4030BEY
HCF4030M013TR
HCF4040BEY
HCF4040M013TR
HCF4042BEY
HCF4042M013TR
HCF4047BEY
HCF4047M013TR
HCF4049UBEY
HCF4049UM013TR
HCF4050BEY
HCF4050M013TR
HCF4051BEY
HCF4051M013TR
HCF4052BEY
HCF4052M013TR
HCF4053BEY
HCF4053M013TR
HCF4056BEY
HCF4056M013TR
HCF4060BEY
HCF4060M013TR
HCF4066BEY
HCF4066M013TR
HCF4067M013TR
HCF4069UBEY
HCF4069UM013TR
HCF4070BEY
HCF4070M013TR
HCF4077M013TR
HCF4081BEY
HCF4081M013TR
HCF4093BEY
HCF4093M013TR
HCF4094BEY
HCF4094M013TR
HCF4097M013TR
HCF4098BEY
HCF4098M013TR
HCF4099BEY
HCF4099M013TR
HCF4538BEY
HCF4538M013TR
HCF4541BEY
HCF4541M013TR
HCF4555BEY
HCF4555M013TR
HCF4556M013TR
M22100B1

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

ⓒ2012 STMicroelectronics - All rights reserved.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morroco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com