PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/20/12304
1.3 Title of PCN	SPC582B5xE1x (FC60): Assembly and Final Testing Activation in Muar
1.4 Product Category	see list
1.5 Issue date	2020-10-02

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Luca RODESCHINI
2.1.2 Marketing Manager	Matteo MOIOLI
2.1.3 Quality Manager	Alberto MERVIC

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	ST Muar (Malaysia)

4. Description of change		
	Old	New
4.1 Description	Assy and Final Test in ST Malta	Assy and Final Test in ST Muar
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Capacity increase
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Codes

7. Timing / schedule	
7.1 Date of qualification results	2020-09-01
7.2 Intended start of delivery	2020-12-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12304 Validation.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2020-10-02

9. Attachments (additional documentations)

12304 Public product.pdf
12304 Validation.pdf
12304 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	SPC582B50E1AD00X	
	SPC582B50E1CG00X	
	SPC582B60E1CD00X	
	SPC582B60E1MH00Y	

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PRODUCT/PROCESS CHANGE NOTIFICATION

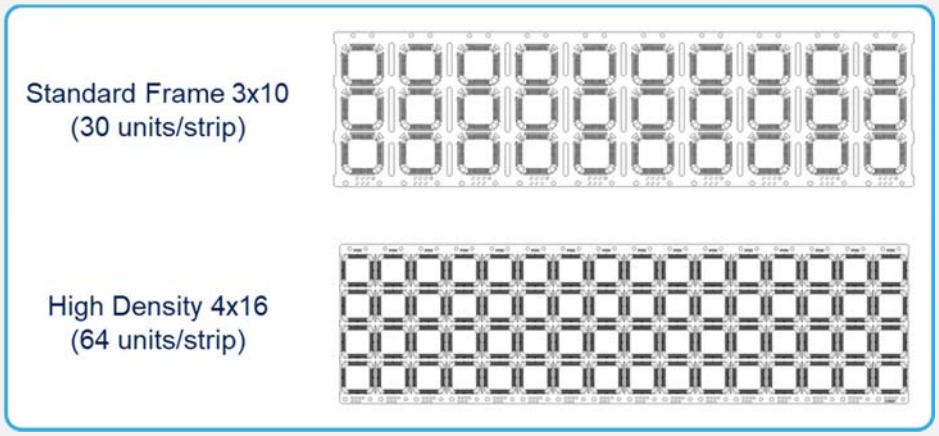
SUBJECT **SPC582B5xE1x (FC60): Assembly and Final Testing Activation in Muar**

IMPACTED PRODUCTS	ST silicon line FC60 assembled in TQFP 64 10x10x1.0 Exposed Pad Package: - SPC582B50E1CG00X - SPC582B50E1AD00X - SPC582B54E1BD00X - SPC582B54E1CG00X - SPC582B60E1CD00X - SPC582B60E1MH00X - SPC582B60E1MH00Y
MANUFACT. STEP	Assembly and Electrical Final Test
INVOLVED PLANT	ST Muar Plant (Malaysia)
CHANGE REASON	Service – Capacity Improvement

CHANGE DESCRIPTION	Transfer of Back End related activities from ST Malta to ST Muar plant, including both Assembly and electrical Final Test
	
	Assembly transfer includeds specific product's improvements linked to new solutions and processes avaliability, such as:
	
	- Package Bill of Material:
	  o move to High Density (HD) leadframe (different supplier)
	  o move to 0.7mil wires diameter
	- Molding Process:
	  o move to central top gate resin injection
	  o move to new molding compound (Sumitomo EME-G700SLS)
	- Marking: re-layout and addition of 2D identifier.
	
	Final Test transfer does not concern changes in test flow or equipment

As far as assembly is concerned, additional details are here below provided.

High Density (HD) Leadframe: increased number of units per strip, from 30 to 64 units/strip.

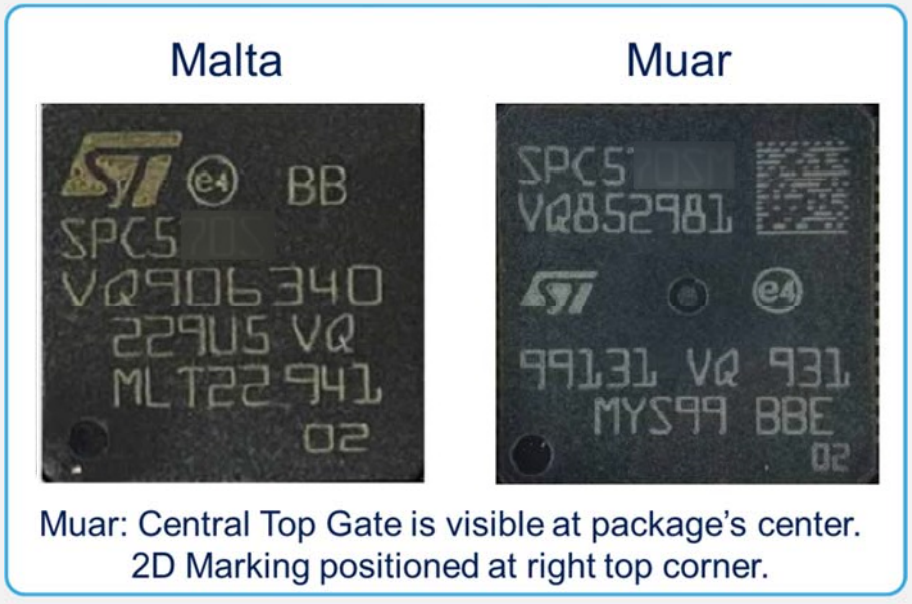


Unit level drawing (pad size, etc.) remains unchanged.

Central Top Gate Mold Injection: reduces stress and possible wire sweeping during molding process.

2D Marking: improves product's internal traceability.

Both changes are visible on package as shown:



Muar: Central Top Gate is visible at package's center.
2D Marking positioned at right top corner.

TRACEABILITY

New Finished Good (internal part number) code and Date Code

VALIDATION

Validation report included in this communication based on ZVEI (AEC-Q100/Q006) recommendations reported in the following table:

x	SEM-PA-08	Change of wire bonding	P	P	Material, diameter, change in bonding diagram and / or change in process resulting in a new technology.	e.g change from Au to Cu material e.g change from 25µm to 23µm diameter e.g change from single to double bond e.g change from stitch bond to stitch on ball bond.	C	**A:** In case of bond diagram change and EM evaluated on component level. Please also check changes described under **SEM-EQ-01**.
x	SEM-PA-11	Change of mold compound / encapsulation material	P	P	Change of mold compound / encapsulation material.	e.g change to green mold compound e.g change of filler particles	C	B: impact on thermo-mechanical stress cau mold compound, interconnecting technolog anticipated (specific for Power Devices). B: for wave soldered devices A: in case of high frequency signals (> 3GHz assessed if possible changes in permeability compound could affect signal behavior (e.g. processor).
x	SEM-PA-13	Change of product marking	I	P	Change of marking on device and / or change in process resulting in a new technology. **(I):** If change does not influence the integrity of the final product. **(P):** If impact on product integrity is anticipated.	**(I):** e.g. change of appearance (additional marking) **(P):** e.g. change from inked marking to laser marking e.g. marking of pin 1	B	
x	SEM-PA-16	Change of direct material supplier	--	P	Change of suppliers for direct materials which are used in assembly process (BOM). **(--):** If change does not influence the integrity of the final product. **(P):** If impact on product integrity is anticipated.	**(--):** e.g. change of wire material supplier. **(P):** e.g. change to new mold compound supplier e.g. additional leadframe supplier with specific leadframe manufacturing technology	C	Please check if material is changed!
x	SEM-PA-18	Move all or parts of production to a different assembly site.	P	P	Assembly transfer or relocation. Includes transfer as well as additional site.	e.g. dual source / lab strategy	C	**A** or **B**: impact on other type of changes de **PROCESS ASSEMBLY** and **SEM-EG**
x	SEM-PA-21	Molding / Encapsulation process	--	P	Change in process technique for molding / encapsulation. **(--):** If the change in process does not influence the integrity of the final product. **(P):** If impact on product integrity is anticipated.	**(--):** e.g. tuning within process specification	C	Check if any other type of process change is the transfer
		PACKING/SHIPPING						
		EQUIPMENT						
		TEST FLOW						
x	SEM-TF-01	Move of all or part of electrical wafer test and/or final test to a different test site.	P	P	Tester transfer or relocation. Check impact on SEM-AN-01 Includes transfer as well as additional site	Dual source strategy	C	Check if any other type of process change is the transfer

	With reference to the above qualification plan, following trials are not performed: - ELFR: silicon related, not applicable to assembly changes; - EM: silicon related, not applicable to assembly changes; - LI: not applicable to surface mount packages; - SC: not applicable to microcontrollers; - PTC: not applicable. Electrical Final Test transfer validation is based on standard correlation exercise (data comparison)
CURRENT PRODUCTS	Upon completion of the transition phase, products will be produced in Muar Plant only
REPORT	12304 Validation.pdf

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : SPC582B5xE1x (FC60): Assembly and Final Testing Activation in Muar

PCN Reference : ADG/20/12304

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

SPC582B60E1MH00Y	SPC582B54E1BD00X	SPC582B50E1CG00X
SPC582B50E1AD00X	SPC582B60E1CD00X	SPC582B54E1CG00X

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RELIABILITY REPORT

ADG – Q&R Digital Products

RR004920_01

Chorus1M eTQFP64 Muar–M40

Reliability Report Chorus1M eTQFP64 Muar Assy M40

FAB transfer

General Information	
Product Line	*FC60*
Product Description	*Chorus1M*
Product Group	*ADG*
Product division	*ADS*
Silicon process technology	*CMOS M40*

Locations	
Wafer fab location	*Crolles 2*

Final Assessment	
Reliability assessment	*Chorus1M eTQFP64 assembled in Muar is qualified according to AEC-Q100 rev.H and AEC-Q006 rev.A.*

DOCUMENT HISTORY

Version	Date	Author	Comment
1.0	31/08/2020	P.Epigrafi	First release

RELEASED DOCUMENT

Auth: P.Epigrafi

Approved: M.De Tomasi **Date: 31/08/2020** **Page: 1 of 13**

RELIABILITY REPORT

ADG – Q&R Digital Products **RR004920_01** **Chorus1M eTQFP64 Muar–M40**

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the reliability trials results for Chorus1M eTQFP64 assy transfer from Malta to Muar.
Chorus1M eTQFP64 product diffused in Crolles and assembled in Malta is in mass production since 2017.

Purpose of the change is to transfer Back End site from ST Malta to ST Muar plant, including both assembly and electrical final test.
Assembly transfer includes specific product improvements linked to new solutions and processes availability, such as:

- Package Bill of Material:
  - change from standard matrix to High Density (HD) matrix leadframe (different supplier) with increased number of units per strip. Unit level drawing (pad size, etc.) remains unchanged
  - change wire diameter from 0.8mils to 0.7mils
  - change of molding compound
- Molding Process: change to central top gate resin injection with the purpose to reduce stress and wire sweeping during molding process.

BOM comparison between Malta and Muar assy is reported in table at paragraph 1.4.

Assy reports are available for all qualification lots.

The qualification exercise for this change is in line with ZVEI Delta Qualification Matrix (ESD CDM performed in addition to ZVEI Requirements according to internal common practice) and it is in respect of AEC-Q100 rev.H and AEC-Q006 rev.A for copper wire qualification.

1.2 Conclusions

Chorus1M eTQFP64 assembled in Muar is qualified according to AEC-Q100 rev.H and AEC-Q006 rev.A.

1.3 Wafer fab information

DIE FEATURES	
Product Code	*FC60*
Diffusion Site	*Crolles 2*
Wafer Diameter (inches)	*12*
Process Technology	*CMOS M40*
Passivation	*PSG + Nitride*
Die finishing back side	*Lapped Silicon*

1.4 Package outline/Mechanical data

	eTQFP64 Malta Assy	*eTQFP64 Muar Assy*
Package Description	*TQFP-EP 64 10X10X1.0 ExpadDown*	*TQFP-EP 64L 10X10X1.0 ExpadDown*
Assembly Site	*ST KIRKOP – MALTA*	*ST MUAR*
Die Attach material	*QMI9507*	*QMI9507*
Molding compound	*G700LS*	*G700SLS*
Substrate/Leadframe	*Standard Pre-plated*	*HD Pre-plated*
Wires bonding materials/diameters	*Cu 0.8mil*	*Cu 0.7mil*

1.5 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	**:**	ST MUAR
Tester	**:**	Teradyne J750

2 RELIABILITY PLAN AND TESTS RESULTS

2.1 Conditions

Room test temperature is 25°C
Hot test temperature is 150°C
Cold test temperature is -40°C

2.2 Tables entry legend

Symbol	How to read
☐	Action or condition has not to be considered
☒	The action/condition has been done/applied during the trial
N.P.	The trial or readout is not in the Qualification Plan and thus has not been performed
N.A.	Not applicable
N.C.	Trial not completed yet

2.3 Accelerated Environmental Stress Test (Q100 Group A)

Test			Step	Results eTQFP64	Notes
N	TEST NAME	CONDITIONS [SPEC]			
A1	**Pre Conditioning MSL 3**	[J-STD-020] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Die visual inspection post trial ☒ 100 Temperature Cycles 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp	**Pre/Post**	0/231 x 3	
A2	**THB** Temperature Humidity Bias	[JESD22-A101/A110] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=85°C, 85%RH, 1000hrs 2000hrs AEC-Q006	**2000 hrs**	0/77x 3	

A3.a	**THS** Temperature Humidity Storage	[JESD22-A101/A110] ☒ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post) ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=85°C, 85%RH, 1000hrs	**1000 hrs**	N.P.	
A3.b	**AC** Autoclave	[JESD22-A102/A118] ☒ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section P=2.08atm Ta=121°C, 96hrs	**96 hrs**	0/77x 3	
A4	**TC** Temperature Cycling	[JESD22-A104] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=-55°C /+150 °C, 1000cyc 2000cyc AEC-Q006	**2000cyc**	0/77x 3	

A5	**PTC** Power Temperature Cycle	[JESD22-A105] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold Ta=-40°C /+125 °C 1000 cyc 2000cyc AEC-Q006	**2000 cyc**	N.P.	Not required on Chorus1M
A6	**HTSL** High Temperature Storage Lifetime	[JESD22-A103] ☐ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☐ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta= 150ºC, 1000hrs 2000hrs AEC-Q006	**2000hrs**	0/77x 3	

2.4 Accelerated Lifetime Simulation Test (Q100 Group B)

Test			Step	Results	Notes
N	TEST NAME	CONDITIONS [SPEC]		Lot 1	
B1.a	**HTOL** High Temp. Operating Life	[JESD22-A108] ☒ After Jedec PC MSL3 ☒ After 1k W/E cyc @125°C ☒ Testing at Room, Hot, Cold ☒ Drift Analysis on Key parameters Ta=125ºC, VDD_HV=5.5V, VDD_LV=1.44V 168hrs (1000hrs monitor)	**168 hrs**	N.P. 0/77 x 1 Chorus4M eTQFP64 assembled in Muar	Similarity with Chorus4M eTQFP64 (Muar Assy)
B1.b	**LTOL** High Temp. Operating Life	[JESD22-A108] ☐ After Jedec PC MSL3 ☒ After 1k W/E cyc @125°C ☒ Testing at Room, Hot, Cold ☒ Drift Analysis on Key parameters Ta=-40ºC, VDD_LV=1.44V 1000hrs	**1000hrs**	N.P.	

RELIABILITY REPORT

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B2	**ELFR** Early Life Failure Rate	[AEC Q100-008] ☒ Testing at Room, Hot Ta= 125ºC, Tj=150°C BI+24 hrs	**BI +24hrs**	N.P.	Silicon stress trial, not significant for assembly changes. Line Stress performed instead
B3.1	**HTDR** High Temp. Data Retention	[AEC Q100-005] ☒ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ After 1k W/E cyc @125°C ☒ Vth Drift Analysis All0, Ta=150ºC, 1000hrs (2000hrs *monitoring*)	**2000 hrs**	N.P.	
B3.2a	**FET @25°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 25ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
B3.2b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	
B3.3a	**FET @125°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 125ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
B3.3b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	
B3.4a	**FET @-40°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= -40ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
B3.4b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	

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RELIABILITY REPORT

ADG – Q&R Digital Products **RR004920_01** **Chorus1M eTQFP64 Muar–M40**

B3.5	**Read Disturb**	After 10 W/E cyc @125°C Ta= 125ºC; 4,5V Stress <1ppm after 6000hrs with ECC	**Final**	N.P.	
B3.6	**Read Disturb**	After 10k W/E cyc @125°C Ta= 125ºC; 4,5V Stress <1ppm after 1 sec with ECC	**Final**	N.P.	

Auth: P.Epigrafi

2.5 Package Assembly Integrity Test (Q100 Group C)

Test			Step	Results	
N	TEST NAME	CONDITIONS [SPEC]		eTQFP64	
C1	**WBS** Wire Bond Shear	[AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices	**Final result**	Passed	
C2	**WBP** Wire Bond Pull	[MIL-STD883 method 2011] 30 bonds x 5 devices	**Final result**	Passed	
C3	**SD** Solderability	[JEDEC JEDES22-B102] > 95% lead coverage	**Final result**	Passed	
C4	**PD** Physical Dimension	[JEDEC JEDES22-B100 and B108]	**Final result**	Passed	
C5	**SBS** Solder Ball Shear	[AEC Q100-010]	**Final result**	N.A.	
C6	**LI** Lead Integrity	[JEDEC JEDES22-B105]	**Final result**	N.A.	

2.6 Die Fabrication Reliability Test (Q100 Group D)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
D1	**EM** Electromigration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D2	**TDDB** Time Dependent Dielectric Breakdown	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D3	**HCI** Hot Carrier Injection	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D4	**NBTI** Negative Bias Temperature Instability	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D5	**SM** Stress Migration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification

RELIABILITY REPORT

ADG – Q&R Digital Products **RR004920_01**

Chorus1M eTQFP64 Muar–M40

2.7 Electrical Verification Test (Q100 Group E)

Test			Step	RESULTS	Notes
N	**TEST NAME**	**CONDITIONS** [AEC Q100]			
E2	**ESD HBM**	HBM = 2kV	**Final result**	N.P.	
E3	**ESD CDM**	CDM = 500V / 750V corner only	**Final result**	PASSED 0/3 per V level	
E4	**LU**	Current Injection Power supply sequence Overvoltage on power supply @Room & Hot	**Final result**	N.P.	
E5	**ED** Electrical Distribution	[AEC Q100-009] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	DONE	
E6	**FG** Fault Grading	[AEC Q100-007] FG shall be = or > 90% for qual units	**Final result**	DONE	
E7	**CHAR** Characterization	[AEC Q103] Performed on new technologies and part families. ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	N.P.	
E9	**EMC** Electromagnetic Compatibility	[SAE J1752/3 – radiated Emission]	**Final result**	N.P.	
E10	**SC** Short Circuit Characterization	[AEC Q100-012] Applicable to all smart power devices. This test and statistical evaluation shall be performed per agreement between user and supplier on a case-by-case basis.	**Final result**	N.A.	
E11	**SER** Soft Error Rate	[JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3] Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed	**Final result**	DONE	Process qualification
E12	**LF** Lead (Pb) Free [AEC Q005]	/	/	YES	

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2.8 Defect Screening Test (Q100 Group F)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
F1	**PAT** Process Average testing	[AEC Q101]	**Final result**	IMPLEMENTED	
F2	**SBA** Statistical Bin/Yield Analysis	[AEC Q102]	**Final result**	IMPLEMENTED	

3 REVISION TRACKING

Rev 1.0

1. First Release