PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data

1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	ADG/20/12124
1.3 Title of PCI	L9396 (UAJ6): Termination of Finished Good code L9396-1(BB silicon)
1.4 Product Category	L9396
1.5 Issue date	2020-04-27

2. PCI Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Alberto DA DALT
2.1.2 Marketing Manager	Marco Antonio FORESTIERO
2.1.3 Quality Manager	Marcello Donato MENCHISE

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	(Not Defined)	ST Muar (Malaysia)

4. Description of change

	Old	New
4.1 Description	Active Finished Good Codes: L9396-1 (BB Silicon) L9396-4 (CB Silicon)	Active Finished Good Codes: L9396-4 (CB Silicon)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Different pin out: pin 53 is VDD on L9396-1 FG, while it is shorted to GND on L9396-4	

5. Reason / motivation for change

5.1 Motivation	Product Improvement in terms of functional safety
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change

6.1 Description	Finished Good L9396-1 (BB silicon version) terminated Finished Good L9396-4 (CB silicon version) replacement

7. Timing / schedule

7.1 Date of qualification results	2020-04-21
7.2 Intended start of delivery	2020-04-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	12124 Validation .pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2020-04-27

9. Attachments (additional documentations)

12124 Public product.pdf
12124 Validation .pdf
12124 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L9396	

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PRODUCT/PROCESS CHANGE INFORMATION

SUBJECT **L9396 (UAJ6): Termination of Finished Good code L9396-1(BB silicon)**

IMPACTED PRODUCTS	L9396
MANUFACTURING STEP	NA
INVOLVED PLANT	NA
CHANGE REASON	Product Improvement in terms of functional safety
CHANGE DESCRIPTION	Finished Good L9396-1 BB silicon version will be terminated, only Finished Good L9396-4 linked to CB Silicon will remains active. NOTICE Different pinout: pin 53 is VDD on L9396-1 FG, while it is shorted to GND on L9396-4
TRACEABILITY	Finished Good L9396-1 (BB silicon version) terminated Finished Good L9396-4 (CB silicon version) replacement
VALIDATION	Finished Good L9396-4 (CB silicon version) already in production qualification report included to this communication
SAMPLES	Available on demand

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : L9396 (UAJ6): Termination of Finished Good code L9396-1(BB silicon)

PCI Reference : ADG/20/12124

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

L9396		

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Reliability Report

L9396 (UAJ6)

New Version

General Information	
Commercial Product	*: L9396*
Product Line	*: UAJ6*
Product Description	*: Multiple Power Supply IC*
Package	*: TQFP64EP (10x10x1mm)*
Silicon Technology	*: BCD8SAUTO*
Division	*: PTS*

Traceability	
Diffusion Plant	*: ST Agrate Brianza (AG8, R2) – Italy*
Assembly Plant	*: ST Muar – Malaysia*

Reliability Assessment	
Passed	☒
Failed	☐
Investigation required	☐

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	28 Sep 2016	R. Alberti	First release for CA cut
1.1	11 Oct 2016	R. Alberti	Updated with CB results
1.2	17 Oct 2016	R. Alberti	Updated with DPA

APPROVED BY: **G. CARLINO**

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

This report presents the results obtained after the reliability evaluation on UAJ6-CA and –CB cuts.
UAJ6 is diffused in BCD8SAUTO in ST Agrate and assembled in TQFP 64 10x10x1.0 1.0 ExpadDown in ST Muar.
The evaluation was carried out on one CA lot, both die- and package-oriented evaluations were performed, and on one CB lot, ESD/LU test only. Details on the next pages.

Refer also to Reliability Report *RR000216CS2039* for activities performed on previous cuts.

1.2 Reliability Test Plan

All reliability tests done (reported with "Y" in Table 1) are performed in agreement with ST internal spec 0061692 and AEC Q100 rev. H procedure.
For details on test conditions and spec reference see test results summary at Par.4

TABLE 1

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	(Y/N)
A Accelerated Environment Stress	**PC (JL3)**	Preconditioning (JL3+3 reflow simulation+100 TC)	Y
	THB	Temperature Humidity Bias	Y
	AC	Autoclave at 2atm	Y
	THS	Temperature Humidity Storage	N
	TC	Temperature Cycling	Y
	PTC	Power Temperature Cycling	N
	HTSL	High Temperature Storage Life	Y
B	**HTOL**	High Temperature Operating Life	Y
	HTRB*	High Temperature Reverse Bias	Y
	ELFR	Early Life Failure Rate	N
	EDR	Electrical Data Retention for NVM	N
C Package Assembly Integrity	**WBS**	Wire Bond Shear	Y
	WBP	Wire Bond Pull	Y
	SD	Solderability	Y
	PD	Physical Dimension	Y
	SBS	Solder Ball Shear	N
	LI	Lead Integrity	Y
E Electrical Verification	**ESD (HBM)**	Electrostatic Discharge (Human Body Model)	Y
	ESD (CDM)	Electrostatic Discharge (Charged Device Model)	Y
	LU	Latch Up	Y
	ED	Electrical distribution	Y
	FG	Fault grade	Y
	CHAR	Characterization	Y
	EMC	Electromagnetic Compatibility	Y
	SC	Short Circuit Characterization	N
	SER	Soft Error Rate	N
	LF	Lead(Pb) Free: (see AEC-Q005)	Y
D Die Fabrication Reliability	*Test list is reported in AEC-Q100 table at Par.4*	*Performed during process qualification*	N
F Defect Screening	*Test list is reported in AEC-Q100 table at Par.4*	*To be implemented starting from first production lot*	N
G Cavity Package Integrity	*Test list is reported in AEC-Q100 table at Par.4*	*N/A: not for plastic packaged devices*	N

(*) not required by AEC Q100

1.3 Conclusion

All reliability tests have been completed. Neither functional nor parametric rejects were detected at final electrical testing.
Parameters drift analysis performed on samples submitted to HTOL showed a good stability of the main electrical monitored parameters. Drifts highlighted after HTOL on previous cuts (see Reliability Report *RR000216CS2039*) are not present anymore.
Package oriented tests have not put in evidence any criticality.
ESD & Latch-Up are in accordance with ST and Customer spec.

Based on the overall results obtained, we can give a positive judgment on the reliability evaluation of UAJ6-CA and -CB (L9396) diffused in ST Agrate Brianza Italy (AG8, R2) and assembled in ST Muar Malaysia (MUAR), performed in agreement to AEC_Q100 Rev.H specification Grade 1.

2 DEVICE/TEST VEHICLE CHARACTERISTICS

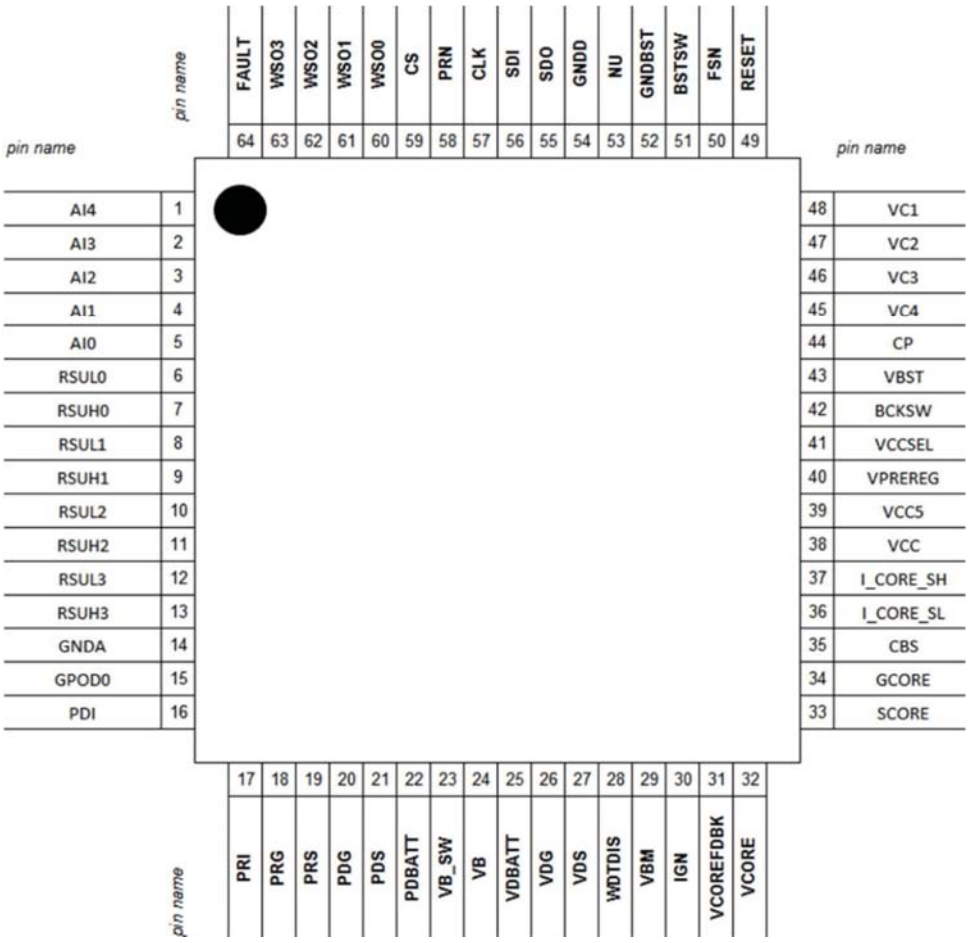
2.1 Generalities

The L9396 is an integrated power management System Basis Chip targeting a large spectrum of automotive electronics applications, in particular ABS, EPS and Transmission, compatible with single (12V) battery system.
It combines a switch mode power supply for pre-regulation together with 3 independent integrated linear regulators and a powerful configurable regulator for µC supply that can operate either in buck or linear mode with an external FET.
The device also integrates a 4-channel flexible interface for Wheel Speed Sensor or tracking regulation, 2 configurable pre-drivers for fail safe and motor pump, 1 configurable general purpose outputs, wake-up detection circuitry, advanced fail-safe functionality, watchdog control and system monitoring.
The boost regulator (optionally enabled) is intended to sustain cold cranking pulses, stop&start and weak battery conditions, while the buck pre-regulator drastically improves the power efficiency and CO_2 emissions.
Different combinations enable to supply the system microcontroller and external peripheral loads and sensors with wide current ranges and adjustable voltage levels.
In addition, the L9396 provides enhanced system standby functionalities.

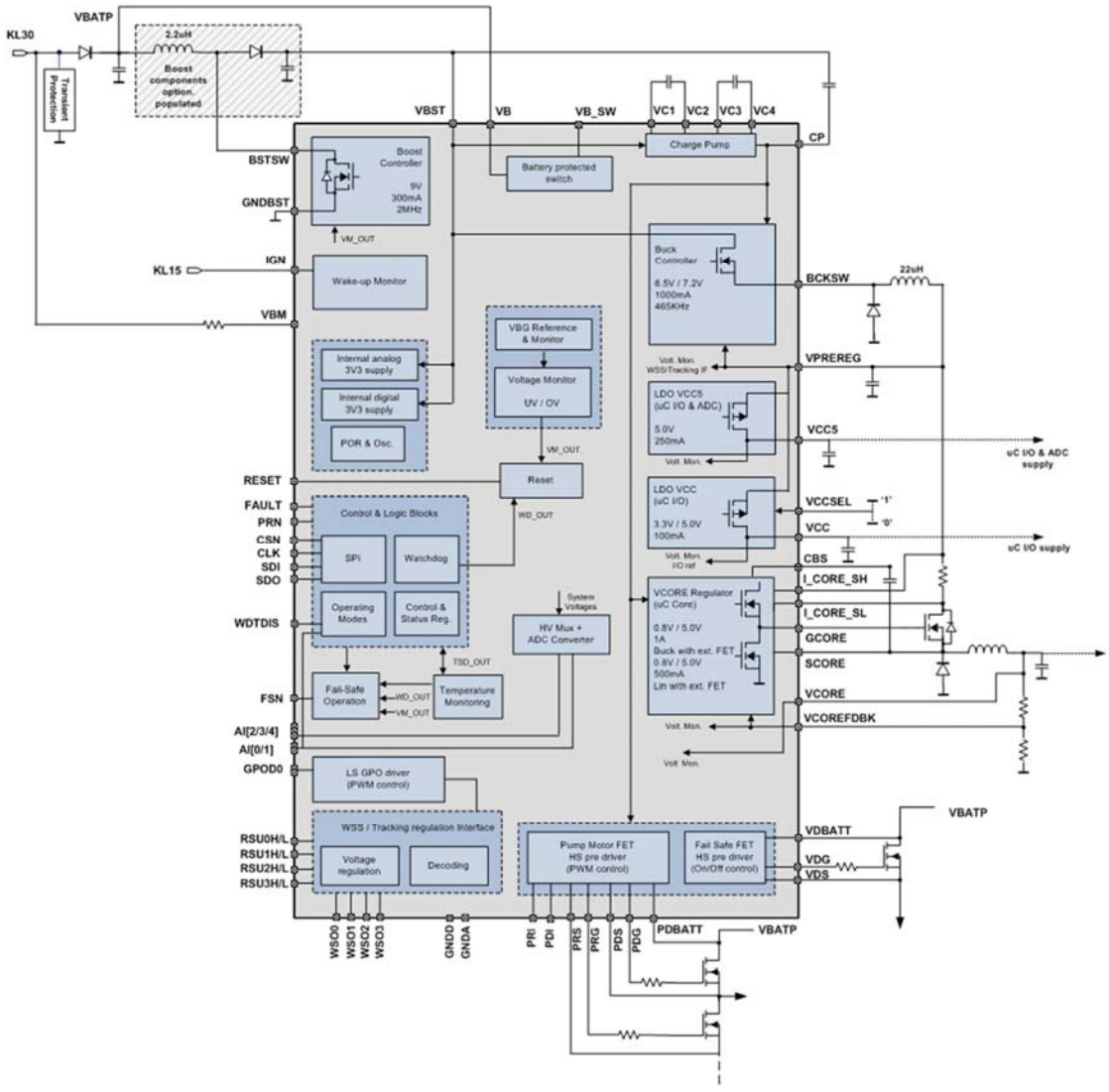
Features

- Integrated boost regulator, 9V, 300mA, 2MHz (opt. populated diode & inductor) for deep cranking pulse (Stop&Start) & weak battery conditions
- Integrated buck pre-regulator, 6.5V / 7.2V, 1A, 465KHz
- Integrated LDO, 5V, 250mA for µC I/O and ADC supply
- Integrated configurable LDO, 3.3V / 5V, 100mA for µC I/O supply
- Configurable and programmable regulator with external FET, 0.8V to 5V for µC core supply
  - up to 1A in buck configuration
  - up to 750mA in linear configuration
- Four channel configurable remote sensor interface
  - wheel speed sensor protocol
  - tracking regulator supply (3.3V – 5V)
  - reverse battery protection and integrated digital decoding
- High-side pre-drivers for fail safe (On/off control) and for motor pump (PWM control)
- SPI communication bus
- Configurable and programmable double watchdog (Q&A WD and temporal WD)
- Low-side general purpose output with programmable PWM control
- Integrated 10-bit ADC with system diagnostics
- Voltage monitoring UV/OV on all regulated rails
- Temperature monitoring and thermal shutdown
- Operating voltage: V_{BATP}: 4.5V to 19V with boost; 6V to 19V without boost
- Ambient temperature range: -40°C to 135°C

2.2 Pin connection



2.3 Block diagram



2.4 Bonding diagram

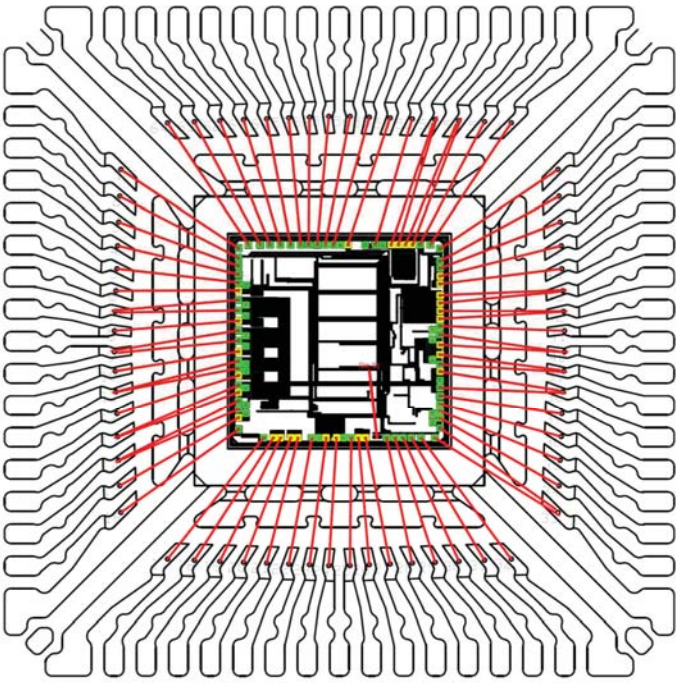
BLANK BOND DIAGRAM FOR LINE: **UAJ6C - RDL**

PKG: **9I**

TOTAL NUMBER OF WIRES : 77

PAD SIZE 4.5x 4.5 mm. / 0.177 x 0.177 Inch

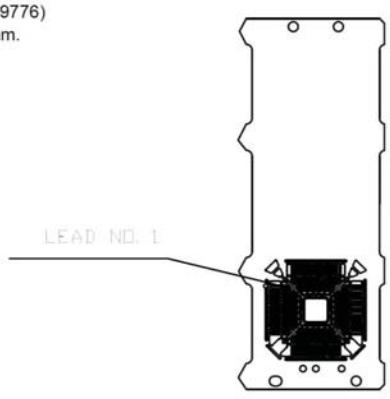
Scale 1mm



TQFP 10X10 64L EP
LF. CODE: 5FT18805 (REF.7469776)
Tot. Wires Lenght: 183.04354 mm.

Std Pads

Critical Pads



2.5 Traceability

2.5.1 Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	ST Agrate Brianza – Italy
Wafer diameter (inches)	8”
Silicon process technology	BCD8SAUTO
Die finishing front side (passivation)	HDP/TEOS/SiN/Polyimide
Die finishing back side	LAPPED SILICON
Die area (Stepping die size)	3470µm x 3350µm
Metal levels/Materials	5 / Ti, TiW, AlCu, TxTN, Cu, NiPd

2.5.2 Assembly information

Assembly Information	
Assembly plant location	ST Muar – Malaysia
Package code description	TQFP 64 10x10x1.0 1.0 ExPad Down
Leadframe/Substrate	FRAME TQFP 64L 10SQ
Die attach material	GLUE LOCTITE ABLESTIK QMI9507
Wires bonding materials/diameters	Cu 1.2 mil
Molding compound	SUMITOMO EME-G700LS

2.5.3 Reliability testing information

Reliability Testing Information	
Reliability laboratory location	ST Cornaredo (Castelletto) – Italy
Electrical testing location	ST Agrate Brianza – Italy
Tester	LTX

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Diffusion Lot	Assy Lot/ Trace Code	Silicon Revision	Note
1	A607476	996181M601	CA	–
2	A607478	9963329V	CB	ESD/LU only

3.2 Test plan and results summary

For Automotive IC.'s, test plan results are summarized in the AEC-Q100 template rev.H with additional STM test conditions as reported below. Revision of test method reference is the one active at the date of reliability test trial

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation Peak Reflow Temp= 260°C Testing at Room 100 Temperature Cycles	APPLIED MSL = Before AC, TC, THB and HTOL			Lot 1: 0 / 308	
THB	A2	JESD22 A101	Ta=85°C, 85%RH, Duration= 1000hrs After PC Testing at Room Testing at Hot Internal Inspection	1	77	77	Lot 1: 0 / 77	

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
AC	A3	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs After PC Testing at Room Internal Inspection	1	77	77	Lot 1: 0 / 77	
TC	A4	JESD22 A104	Ta=-55°C /+150 °C Duration= 1000 cyc Robustness= 2000 cyc After PC Testing at Room Testing at Hot C/T-SAM pre / post WBP (first / second bond) Internal Inspection	1	77	77	Lot 1: 0 / 77	Robustness on Lot 1
PTC	A5	JESD22 A105	Ta=-40°C /+125 °C Duration=1000 cyc of 1 hr	–	–	–	–	
HTSL	A6	JESD22 A103	Ta= 150°C Duration= 1000hrs Robustness= 2000hrs Testing at Room Testing at Hot WBP (first / second bond)	1	77	77	Lot 1: 0 / 77	Robustness on Lot 1

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	Ta= 95°C (TJ=160°C) Duration= 1000hrs Robustness= 2000hrs These are the min values. Testing at Room Testing at Cold Testing at Hot Drift Analysis	1	77	77	Lot 1: 0 / 77	
HTRB		JESD22 A108	Ta= 135°C (TJ=150°C) Duration= 1000hrs Testing at Room	1	45	45	Lot 1: 0 / 45	
ELFR	B2	AEC-Q100-008	Burn-in conditions with -Tj=150°C (Ta max=125°C) -Duration=48hrs	–	–	–	–	Burn-in data
EDR	B3	AEC-Q100-005		–	–	–	–	N/A

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	bonds	All measurement within spec limits	Assembly data
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	bonds	All measurement within spec limits	Assembly data
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	All measurement within spec limits	Assembly data
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	All measurement within spec limits	Assembly data
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	3	50 balls		All measurement within spec limits	Assembly data (only for BGA)
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through- hole only; 10 leads from each of 5 devices	1	50 leads		All measurement within spec limits	Assembly data (only for TTH)

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Data, test method and criteria should be available upon request	-	-	-	PASSED	Process qualification data
TDDB	D2	JESD35	Data, test method and criteria should be available upon request	-	-	-	PASSED	Process qualification data
HCI	D3	JESD60 & 28	Data, test method and criteria should be available upon request	-	-	-	PASSED	Process qualification data
NBTI	D4	JESD90	Data, test method and criteria should be available upon request	-	-	-	PASSED	Process qualification data
SM	D5	JESD61, 87, & 202	Data, test method and criteria should be available upon request	-	-	-	PASSED	Process qualification data

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP E - ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test: All parametric and functional tests	All	All	All	Passed	
HBM	E2	AEC-Q100-002	Target HBM=+/-2KV all pins; +/-4KV global pins Testing at Room Testing at Hot	1	See test method		Passed for CA and CB	
CDM	E3	AEC-Q100-011	Target CDM=+/-750V on corner pins; +/- 500V all others Testing at Room Testing at Hot	1	See test method		Passed for CA and CB	
LU	E4	AEC-Q100-004	Current Injection Class II - Level A (+/- 100mA) Testing at Room Testing at Hot	1	6	6	Passed for CA and CB	
LU	E4	AEC-Q100-004	Overvoltage Class II - Level A (1,5 x Vmax) Testing at Room Testing at Hot	1	6	6	Passed for CA and CB	
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)	3	30	90	Passed	Covered by Electrical Characterization
FG	E6	AEC-Q100-007	Fault Grading: FG shall be = or > 90% for qual units	-	-	-		
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	Passed	Covered by Electrical Characterization
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1	1	1		Done at application level
SC	E10	AEC Q100-012	Short Circuit Characterization	0	10	0		
SER	E11	JESD89-1 JESD89-2 JESD89-3	Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications	0	3	0		
LF	E12	AEC-Q005	Lead(Pb) Free: (see AEC-Q005)	-	-	-		Covered by Test group A & C

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)

TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside Avg.	Not performed on qualification lots. It will be implemented starting from first production lot
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Not performed on qualification lots. It will be implemented starting from first production lot

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS
(for Ceramic Package testing only)

MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	1	15	15	of	For cavity package only
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	1	15	15	of	For cavity package only
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	1	15	15	of	For cavity package only
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	1	15	15	of	For cavity package only
DROP	G5	----------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	1	5	5	of	For MEMS cavity device only
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	1	5	5	of	For cavity package only
DS	G7	MIL-STD-883 Method 2019	Die Shear:	1	5	5	of	For cavity package only
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	1	3	3	of	For cavity package only