PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data		
1.1 Company		STMicroelectronics International N.V
1.2 PCI No.		ADG/20/11983
1.3 Title of PCI		Microcontrollers (M10): Lead Locking Tape (LLT) introduction on LQFP-100 14x14x1.4 Package
1.4 Product Category		see list
1.5 Issue date		2020-02-05

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Luca RODESCHINI
2.1.2 Marketing Manager	Selica RUSSI
2.1.3 Quality Manager	Alberto MERVIC

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	Same part number of direct materials, same supplier but qualified and used in other ST plant	ST Kirkop (Malta)

4. Description of change		
	Old	New
4.1 Description	No Lead Locking Tape (LLT)	Lead Locking Tape (LLT)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	To reduce or remove the occurrence of possible internal bent leads issues, characterized by intrinsic low detectability
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Datecode

7. Timing / schedule	
7.1 Date of qualification results	2020-01-30
7.2 Intended start of delivery	2020-03-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	11983 Qualification Report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2020-02-05

9. Attachments (additional documentations)

11983 Public product.pdf
11983 Qualification Report.pdf
11983 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	SPC560B50L3B4E0X	
	SPC560B50L3C6E0X	
	SPC560B50L3C6E0Y	
	SPC560B54L3C6E0X	
	SPC560C50L3B4E0X	
	SPC560C50L3C6E0X	
	SPC560D30L3B3E0X	
	SPC560P40L3BEAAY	
	SPC560P40L3CEFAR	
	SPC560P40L3CEFBR	
	SPC560P40L3CEFBY	
	SPC560P44L3BEAAY	
	SPC560P44L3CEFAR	
	SPC560P50L3BEABR	
	SPC560P50L3CEFAR	
	SPC560P50L3CEFAY	

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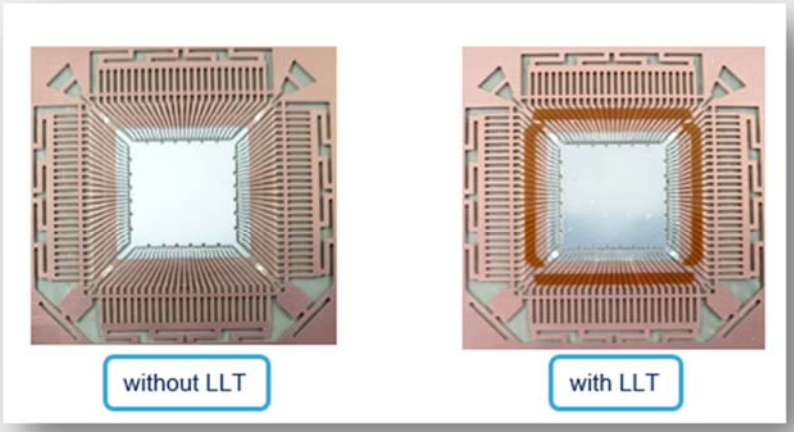
PRODUCT/PROCESS CHANGE INFORMATION

SUBJECT	Microcontrollers (M10): Lead Locking Tape (LLT) introduction on LQFP-100 14x14x1.4 Package
IMPACTED PRODUCTS	M10 technology Microcontrollers assembled in LQFP 100 14x14x1.4 package, corresponding to ST silicon lines: - FB40 - FB50 - FB64 - FP40 - FP50 - FP60 Detailed part numbers list: see attached table
MANUFACTURING STEP	Assembly
INVOLVED PLANT	ST Kirkop Plant (Malta)
CHANGE REASON	Lead Locking Tape (LLT) can be used on high pin count QFP packages to reduce or remove the occurrence of possible internal bent leads issues, characterized by intrinsic low detectability. This solution is a standard for higher pint count packages (such as 144 and 176 leads) and is now extended to the QFP 100 leads configuration whenever applicable. Above mentioned impacted products already adopt this solution in packages with pin counts higher than 100
CHANGE DESCRIPTION	Lead Locking Tape simply consists of a chemically inert tape that is blocking the leads in their original position, securing them during the assembly process steps, as shown in the following picture:



Apart from the addition of the tape, no lead frame modifications are introduced:

Drawings

- dimensions: unchanged
- thickness: unchanged
- tolerances: unchanged

Materials

- base material: unchanged
- surface finishing: unchanged
- suppliers: unchanged

Lead Locking Tape does not concerns lead tips / wires interface

TRACEABILITY

Internal Traceability and Date Code

VALIDATION

No specific item is recalled by ZVEI (AEC-Q100) Delta Qualification Matrix. Considering the type of change and potential failure modes, following qualification plan has been executed:

1. MSL3 + 1000TC
2. 1000hrs HTS
3. MSL3 + AC
4. MSL3+ 1000hrs THB

Validation has been completed positively and solution can be released for production

CURRENT PRODUCTS	Replaced by updated version adopting LLT
REPORTS	See attached Qualification Reliability Report

.

Reliability Report
M10 LQFP100 - Malta
Lead Locking Tape Qualification

General Information	
Product Line	FP40, FP50, FP60, FB40, FB50, FB64
Product Description	Pictus 256K, Pictus512K, Pictus1M, Bolero256K, Bolero512K, Bolero1M5
Product Group	*ADG*
Product division	*ADS*
Silicon process technology	*CMOS M10*

Locations	
Wafer fab location	*Crolles*
Assy Plant	*Malta*

Final Assessment	
Reliability assessment	Qualification of M10 products assembled in LQFP100 14x14 package with LLT completed with positive results

DOCUMENT HISTORY

Version	Date	Author	Comment
1.0	24/01/2020	P.Epigrafi	M10 products LQFP100 LLT qualification results
2.0	28/01/2020	P.Epigrafi	Typo correction. Added details of qualification strategy

RELEASED DOCUMENT

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the results of reliability trials performed to qualify the introduction of Lead Locking Tape (LLT) on M10 products assembled in Malta in LQFP100 package.

M10 products are currently qualified in Malta according to AEC-Q100 rev.G and AEC-Q006 rev.A.

LLT is already used in production on M10 products assembled in high pin number QFP packages. The reason to introduce LLT on 100L package is due to improvement in the manufacturability and overall improved quality.

The change does not have an impact on frame geometry, frame material and finishing.

LLT materials and suppliers are the same already qualified for production on M10 LQFP176 and LQFP144.

Three different suppliers of Leadframe with LLT have been qualified (Shinko, Heasung - HDS, CWTC).

LLT introduction on M10 products assembled in Malta in LQFP100 package has been qualified with reliability trials performed on:

- Pictus512K (FP50) LQFP100 – Shinko Supplier
- Pictus512K (FP50) LQFP100 – Heasung (HDS) Supplier
- Pictus256K (FP40) LQFP100 – CWTC Supplier

Other M10 products assembled in Malta in LQFP100 package (Pictus1M, Bolero256K, Bolero512K, Bolero1M5) have been qualified by similarity.

LLT introduction does not concern lead tips and wire interfaces, so the qualification exercise to qualify the change is in respect of AEC-Q100-Rev.G.

For each lot, qualification trials performed are:

- HTS 1000hrs
- Pre-conditioning + 1000cyc Thermal Cycles
- Pre-conditioning + AC 96hrs
- Pre-conditioning + THB 1000hrs

1.2 Conclusions

All qualification trials have been completed with positive results.

On the ground of the overall positive results we conclude that M10 products assembled in Malta in LQFP100 with Leadframe with LLT are qualified in compliance with AEC-Q100 rev.G and AEC-Q006 rev.A.

2 TRACEABILITY

2.1 Wafer fab information

DIE FEATURES	
Diffusion Site	*Crolles 2*
Wafer Diameter (inches)	12
Process Technology	*CMOS M10*
Passivation	PSG- Nit UV
Die finishing back side	Lapped Silicon

2.2 Package outline/Mechanical data

Product	**Pictus 512K (FP50)**	**Pictus 512K (FP50)**	**Pictus 256K (FP40)**
Package Description	*LQFP 100 14x14 (Shinko)*	*LQFP 100 14x14 (Heasung)*	*LQFP 100 14x14 (CWTC)*
Assembly Site	*ST KIRKOP – MALTA*	*ST KIRKOP – MALTA*	*ST KIRKOP – MALTA*
Die Attach material	*QMI9507-1A1*	*QMI9507-1A1*	*QMI9507-1A1*
Molding compound	*G700LS*	*G700LS*	*G700LS*
Substrate/Leadframe	*FRAME LQFP 100L 14x14 SpAg*	*FRAME LQFP 100L 14x14 SpAg*	*FRAME LQFP 100L 14x14 SpAg*
Wires bonding materials/diameters	*CuPd 0.7mils*	*CuPd 0.7mils*	*CuPd 0.7mils*

2.3 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	**:**	ST KIRKOP – MALTA
Tester	**:**	Teradyne J750

3 RELIABILITY PLAN AND TESTS RESULTS

3.1 Conditions

Room test temperature is 25°C
Hot test temperature is 150°C
Cold test temperature is -40°C

3.2 Tables entry legend

Symbol	How to read
☐	Action or condition has not to be considered
☒	The action/condition has been done/applied during the trial
N.P.	The trial or readout is not in the Qualification Plan and thus has not been performed

3.3 Accelerated Environmental Stress Test (Q100 Group A)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS [SPEC]		LQFP100 Malta	
1	**PC Pre-Conditioning**	[J-STD-020] ☒ Testing at Room ☒ Testing at Hot ☒ Sonoscan pre / post 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp	**JL3**	0/231 x 3	Trial performed on 2 lots of Pictus512K and 1 lot of Pictus256K AEC-Q006 milestone reached during product qualification
2	**THB** Temperature Humidity Bias	[JESD22-A101/A110] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot Ta=85°C, 85%RH, 1000hrs	**1000 hrs**	0/77 x 3	Trial performed on 2 lots of Pictus512K and 1 lot of Pictus256K AEC-Q006 milestone reached during product qualification

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS [SPEC]		LQFP100 Malta	
3	**AC** Autoclave	[JESD22-A102/A118] ☒ After Jedec PC MSL3 ☒ Testing at Room P=2.08atm Ta=121°C, 96hrs	**96 hrs**	0/77 x 3	Trial performed on 2 lots of Pictus512K and 1 lot of Pictus256K AEC-Q006 milestone reached during product qualification
4	**TC** Temperature Cycling	[JESD22-A104] ☒ After Jedec PC MSL3 ☐ Testing at Room ☒ Testing at Hot ☒ Sonoscan pre / post ☒ WPT post ☒ WBS post Ta=-55°C /+150 °C 1000 cyc	**1000 cyc**	0/77 x 3	Trial performed on 2 lots of Pictus512K and 1 lot of Pictus256K AEC-Q006 milestone reached during product qualification
5	**HTSL** High Temperature Storage Lifetime	[JESD22-A103] ☒ Testing at Room ☒ Testing at Hot Ta= 150ºC, 1000hrs	**1000 hrs**	0/77 x 3	Trial performed on 2 lots of Pictus512K and 1 lot of Pictus256K AEC-Q006 milestone reached during product qualification

3.4 Package Assembly Integrity Test (Q100 Group C)

Test			Step				
N	TEST NAME	CONDITIONS [SPEC]		Pictus512K (Shinko) LQFP100	Pictus512K (HDS) LQFP100	Pictus256K (CWTC) LQFP100	Notes
C1	**WBS** Wire Bond Shear	[AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices	**Final result**	Passed	Passed	Passed	Assy report
C2	**WBP** Wire Bond Pull	[MIL-STD883 method 2011] 30 bonds x 5 devices	**Final result**	Passed	Passed	Passed	Assy report
C3	**SD** Solderability	[JEDEC JEDES22-B102] > 95% lead coverage	**Final result**	Passed	Passed	Passed	Assy report
C4	**PD** Physical Dimension	[JEDEC JEDES22-B100 and B108]	**Final result**	Passed	Passed	Passed	Assy report
C5	**SBS** Solder Ball Shear	[AEC Q100-010]	**Final result**	N.A.	N.A.	N.A.	Assy Report
C6	**LI** Lead Integrity	[JEDEC JEDES22-B105]	**Final result**	N.A.	N.A.	N.A.	Not applicable

4 REVISION TRACKING

Rev2.0
1. Typo correction in introduction page
2. Added details of qualification strategy

Rev 1.0
1. First release

Public Products List

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PCI Title : Microcontrollers (M10): Lead Locking Tape (LLT) introduction on LQFP-100 14x14x1.4 Package

PCI Reference : ADG/20/11983

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

SPC560B50L3C4E0X	SPC560P40L3CEAAR	SPC560B60L3B6E0X
SPC560P44L3BEAAR	SPC560P40L3CEFBR	SPC560B50L3B4E0X
SPC560P44L3BEAAY	SPC560B54L3C6E0X	SPC560D40L3B4E0X
SPC56AP60L3BEAAR	SPC56AP54L3BEFBY	SPC560P54L3BEABY
SPC560P40L3CEFAR	SPC560D40L3C4E0X	SPC560B40L3B4E0X
SPC560P50L3CEFAR	SPC560P44L3CEABR	SPC56AP60L3BEFBY
SPC560B50L3B6E0X	SPC560B54L3B4E0X	SPC560P50L3BEFAR
SPC56AP60L3BEABY	SPC560P50L3BEABY	SPC560P50L3BEFAY
SPC560P60L3CEFAY	SPC560P40L3CEFBY	SPC560C50L3C6E0X
SPC560B60L3C6E0X	SPC560C50L3B4E0X	SPC560P50L3CEFBR
SPC560B40L3C6E0X	SPC560P50L3CEFBY	SPC560P50L3CEFAY
SPC560B50L3C6E0X	SPC560D40L3B3E0Y	SPC56AP60L3BEABR
SPC560P60L3BEABR	SPC560P54L3BEABR	SPC560D30L3B3E0X
SPC56AP60L3BEAAY	SPC560P60L3BEABY	SPC56AP60L3BEFBR
SPC560C40L3C6E0X	SPC560P60L3CEFAR	SPC560B64L3B6E0X
SPC560P40L3BEAAY	SPC56AP54L3BEFBR	SPC560P50L3BEABR
SPC560P44L3CEFAR	SPC560B50L3C6E0Y	SPC560P44L3CEFAY

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