PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/20/11971
1.3 Title of PCN	STM32L5 product improvement
1.4 Product Category	STM32L5 products
1.5 Issue date	2020-05-28

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	TSMC FAB14 (Taiwan)

4. Description of change		
	Old	New
4.1 Description	STM32L5 512K 1. Rev B having following SMPS limitations - Limitation with SMPS transition from HP mode to LP mode (Documented in Errata Sheet: LP mode not recommended) - Limitation with SMPS state which is unpredictable at power-on (Documented in Errata Sheet : The limitation occurrence probability is low, no workaround). Documented in ES0448 - Rev 4 - November 2019 2. Bootloader version (V9.1) AN2606 - Rev 42 - December 2019	STM32L5 512K fixes 1. Rev Z including fixes of SMPS limitations - No more limitation “SMPS regulation loss upon transiting into SMPS LP mode”. - No more limitation “Unpredictable SMPS state at power-on Documented in ES0448 - Rev 5 - April 2020 2. Bootloader version update (V9.2): no functional impact for end user. Documented in AN2606 - Rev 43 - June 2020
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Functionality Improvement	

5. Reason / motivation for change	
5.1 Motivation	STM32L5 512K: Revision Z includes fix of SMPS limitation identified in Revision B
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Tracability ensured by ST internal tools

7. Timing / schedule	
7.1 Date of qualification results	2020-04-15
7.2 Intended start of delivery	2020-06-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	11971 MDG-MCD-RER1620 V1.2 - STM32L552x - STM32L562x - Die 472XXXZ - PCN11971 - Reliability Evaluation Report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2020-05-28

9. Attachments (additional documentations)
11971 Public product.pdf 11971 MDG-MCD-RER1620 V1.2 - STM32L552x - STM32L562x - Die 472XXXZ - PCN11971 - Reliability Evaluation Report.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32L552CCT6	
	STM32L552CCU6	
	STM32L552CET6	
	STM32L552CEU6	
	STM32L552QEI6	
	STM32L552RCT6	
	STM32L552RET6	
	STM32L552VET6	
	STM32L552ZET6	
	STM32L562CET6	
	STM32L562CEU6	
	STM32L562RET6	
	STM32L562ZET6	

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Reliability Evaluation Report

MDG-MCD-RER1620

STM32L552x/L562x (472x66)

New Product Qualification

General Information	
Commercial Product	STM32L552 / L562 xC/E
Product Line	472X66
Die revision	472XXXZ(Cut 2.1)
Product Description	STM32L552 / L562 Family
Package	LQFP20x20 144L, LQFP14x14 100L, LQFP10x10 64L, LQFP7x7 64L, UFBGA7x7 132L, UFQFPN7x7 48L, WLCSP81
Silicon Technology	TSMC Fab14 90 ULL
Division	MDG-MCD
Reliability Maturity Level	20->30

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan
Assembly Plant	ASE, Taiwan. JSCC, China. SC AMKOR ATP3, Philippines. AMKOR ATT1, Taiwan

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	26th Aug 2019	Muriel GALTIER Pascal CARDOSI	MDG-MCD-Q&R Engineer
1.1	13th Feb 2019	Muriel GALTIER Pascal CARDOSI	MDG-MCD-Q&R Engineer
1.2	03th Apr 2020	Muriel GALTIER Pascal CARDOSI	MDG-MCD-Q&R Engineer

APPROVED BY:

VERSION 1.0

Function	Location	Name	Date
Division Q&R Responsible	Rousset	Frederic BRAVARD Dominique GALIANO	16-Oct-2019
Division Quality Manager	Rousset	Pascal NARCHE	27-Nov-2019

VERSION 1.1

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	14-Feb-2020

VERSION 1.2

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	06-Apr-2020

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation on STM32L552/L562 xC/E - Die 472XXXZ.

Test vehicle is described here below:

Product	Process, Package	Diffusion, Assembly plant	*Comments*
STM32L552ZET6	90ULL, LQFP 20x20 144L	TSMC Fab14, SC ASE TAIWAN	LQFP144 Legacy
STM32L552ZET6Q	90ULL, LQFP 20x20 144L	TSMC Fab14, SC ASE TAIWAN	LQFP144 Int SMPS
STM32L552VET6	90ULL, LQFP 14x14 100L	TSMC Fab14, SC ASE TAIWAN	LQFP100 Legacy
STM32L552VET6Q	90ULL, LQFP 14x14 100L	TSMC Fab14, SC ASE TAIWAN	LQFP100 Int SMPS
STM32L552RET6	90ULL, LQFP 10x10 64L	TSMC Fab14, JSCC	LQFP64 Legacy
STM32L552RET6Q	90ULL, LQFP 10x10 64L	TSMC Fab14, JSCC	LQFP64 Int SMPS
STM32L552RET6P	90ULL, LQFP 10x10 64L	TSMC Fab14, JSCC	LQFP64 Ext-SMPS
STM32L552CET6	90ULL, LQFP 7x7 48L	TSMC Fab14, JSCC	LQFP48 Legacy
STM32L552CET6P	90ULL, LQFP 7x7 48L	TSMC Fab14, JSCC	LQFP48 Ext SMPS
STM32L552CEU6	90ULL, UFQFPN 7x7 48L	TSMC Fab14, JSCC	UFQFN48 Legacy
STM32L552CEU6P	90ULL, UFQFPN 7x7 48L	TSMC Fab14, JSCC	UFQFN48 Ext-SMPS
STM32L552QEI6	90ULL, UFBGA 7x7 132L	TSMC Fab14, ATP3	UFBGA132 Legacy
STM32L552QEI6Q	90ULL, UFBGA 7x7 132L	TSMC Fab14, ATP3	UFBGA132 Int SMPS
STM32L552QEI6P	90ULL, UFBGA 7x7 132L	TSMC Fab14, ATP3	UFBGA132 Ext SMPS
STM32L552MEY6Q	90ULL, WLCSP 81L	TSMC Fab14, ATT1	CSP81 Int SMPS
STM32L552MEY6P	90ULL, WLCSP 81L	TSMC Fab14, ATT1	CSP81 Ext SMPS

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32L552/L562 xC/E - Die 472XXXZ, is processed in the 90ULL process from TSMC Fab14 Taiwan plant which is qualified through ORCA 1M - Die 415 (RERMCD1112) for our division.

All packages used for this product are qualified at division level.

The STM32L552x/L562x (Die 472) is based on STM32L4x product family, processed in TSMC90nm technology in FAB14

STM32L486x (die 415): RERMCD1112
STM32L433x (die 435): RERMCD1424
STM32L452x (die 462): RERMCD1526
STM32L496x (die 461): RERMCD1521

The STM32L552/L562 xC/E (Die 472) device is assembled in the following packages already qualified for this product family:

Package	Reference	Assy Plant location
UFBGA7x7 132L	RERMCD1402 / RERMCD1112	AMKOR ATP3
LQFP20x20 144L	RERMCD1312 RERMCD1810	AMKOR ATP1 ASEKH
LQFP14x14 100L	RERMCD1810	ASEKH
LQFP10x10 64L	RERMCD1606	JSCC
LQFP7x7 48L	RERMCD1606	JSCC
UQFN7x7 48L	RERMCD1622	JSCC
WLCSP81	RERMCD1112	AMKOR ATT1

Based on these data, and according to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:
  - Cut1.0: 2 reliability lots to assess the die in UFBGA132 package.
    2 reliability lots to assess the SMPS in LQFP144 package mounted on chipboards
  - Cut2.0: 1 reliability lot to assess the die in UFBGA132 package.
    1 reliability lot to assess the SMPS in LQFP144 package mounted on chipboards
  - Cut2.1: 1 partial reliability lot to assess the die in UFBGA132 package.
    1 reliability lot to assess the SMPS in LQFP144 package mounted on chipboards

- Package Qualification:

The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
LQFP 144	20x20	0.5	1A	Gold	ASEKH	Legacy	CDM, HBM, LU
LQFP 144	20x20	0.5	1A	Gold	ASEKH	Int-SMPS	CDM, HBM, LU
LQFP 100	14x14	0.5	1L	Gold	ASEKH	Legacy	1 reliability lot
LQFP 100	14x14	0.5	1L	Gold	ASEKH	Int-SMPS	CDM
LQFP 64	10x10	0.5	5W	Gold	JSCC	Legacy	CDM
LQFP 64	10x10	0.5	5W	Gold	JSCC	Int-SMPS	CDM
LQFP 64	10x10	0.5	5W	Gold	JSCC	Ext-SMPS	CDM
LQFP 48	7x7	0.5	5B	Gold	JSCC	Legacy	1 reliability lot
LQFP 48	7x7	0.5	5B	Gold	JSCC	Int-SMPS	CDM
UFQFPN 48	7x7	0.5	A0B9(MI)	Gold	JSCC	Legacy	1 reliability lot
UFQFPN 48	7x7	0.5	A0B9(MI)	Gold	JSCC	Ext-SMPS	CDM
UFBGA 132	7x7	0.5	A0G8(PG)	Gold	ATP3	Legacy	CDM
UFBGA 132	7x7	0.5	A0G8(PG)	Gold	ATP3	Int-SMPS	CDM
UFBGA 132	7x7	0.5	A0G8(PG)	Gold	ATP3	Ext-SMPS	CDM, HBM, LU
WLCSP 81	-	0.4	B01H(FY)	-	ATT1	Int-SMPS	CDM
WLCSP 81	-	0.4	B01H(FY)	-	ATT1	Ext-SMPS	CDM

Note: In order to cover all I/O options, ESD HBM & LU trials have been executed for Legacy, Internal SMPS and External SMPS max pin count package option.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the STM32L552 / L562 xC/E - Die 472XXXZ in all packages listed in section 1.2

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

The STM32L552 / L562 xC/E devices are an ultra-low-power microcontrollers family (STM32L5 Series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 110MHz.

For additional information concerning the product behavior, refer to STM32L552/L562 xC/E datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	T14F - TSMC Fab 14
Wafer diameter (inches)	12
Wafer thickness (µm)	775 +/- 25
Silicon process technology	90nm eFlash Generic TSMC
Number of masks	45
Die finishing front side (passivation) materials/thicknesses	USG + NITRIDE, 1.75µm
Die finishing back side Materials/thicknesses	RAW SILICON
Die area (Stepping die size) (µm)	4099.2, 4391
Die pad size (X,Y) (µm)	123, 59
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	Metal 1 TaN/Ta/CuSeed/Cu 0.240µm Metal 2 TaN/Ta/CuSeed/Cu 0.310µm Metal 3 TaN/Ta/CuSeed/Cu 0.310µm Metal 4 TaN/Ta/CuSeed/Cu 0.310µm Metal 5 TaN/Ta/CuSeed/Cu 0.310µm Metal 6 TaN/Ta/CuSeed/Cu 0.850µm Metal 7 AlCu 1.450µm
Die over coating (material/thickness)	No
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	2.1 FITs at qualification date
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm².
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI)	Yes

- Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	
Other Device(s) using same process	STM32L4x, STM32G4x product family, 415, 435, 461, 462, 464, 468, 469, 470.

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 - 1A LQFP 144 20X20X1.4	
Assembly plant name / location	AMKOR ATP1 - PHILIPPINES
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF for LQFP20x20 144L PPF 6.2sq
Lead frame finishing (material)	PPF (e4)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076YB
Wire bonding material/diameter/supplier	GOLD WIRE 0.8MIL
Molding compound material/supplier/reference	Resin SUMITOMO G631HQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 2 - 1A LQFP 144 20X20X1.4	
Assembly plant name / location	ASEKH - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF# A25582 LQ20 144L Pure Tin C7025 6.6sq
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO EME-G631SH
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 3 - 1L LQFP 100 14x14x1.4	
Assembly plant name / location	ASEKH - TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LF# A25516 LQ14 100L Pure Tin C7025 6.6sq Slot
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	GLUE SUMITOMO EPOXY CRM 1076WA
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO EME-G631SH
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 4 - 5W LQFP 64 10x10x1.4	
Assembly plant name / location	JSCC - China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LQ10 64L 207sq Eff slots STMP LF JSCC
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	D/A Ablestik 3230
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 5- 5B LQFP 48 7x7x1.4	
Assembly plant name / location	JSCC - China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	LQFP48L 200sq Eff slots pur tin STMP LF JSCC
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	D/A Ablestik 3230
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO low alpha G631SHQ
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 6 - A0B9 (MI) UFQFPN 7X7X0.55 48L	
Assembly plant name / location	JSCC - China
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/-25
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	Rough Cu LF UQFN48L 5.2sq Groove JSCC
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	Glue Hitachi EN4900GC
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Molding compound material/supplier/reference	SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 7 - A0G8 (PG) UFBGA 7X7X0.6 132L P 0.5 R 12X12	
Assembly plant name / location	AMKOR ATP3 - PHILIPPINES
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 +/-12
Die sawing method	Mechanical Sawing
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	SUBSTRATE FOR UFBGA 7X7 132L
Lead frame finishing (material)	Pure Tin (e3)
Die attach material/type(glue/film)/supplier	DAF Ablestik ATB130U
Wire bonding material/diameter/supplier	GOLD WIRE 0.8 mils
Balls metallurgy/diameter/supplier (BGA/CSP)	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Molding compound material/supplier/reference	MOLDING COMPOUND GE100LFCS
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 8 - B01H (FY) WLCSP 81L P0.4 DIE 472	
Assembly plant name / location	SC AMKOR ATT1 - TAIWAN
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355 +/-25
Die sawing method	LASER GROOVE + STEP CUT
Bill of Material elements	
Balls metallurgy/diameter/supplier (BGA/CSP)	Solder ball SAC405 Diam 230um
Routing/Redistribution layer (RDL) material (CSP)	Copper 6um
PBO passivation material (CSP)	Passivation HD8820
Backside coating material/thickness (CSP)	Back side coating PET film
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 1

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	RSST / ST Rousset GRAL / ST Grenoble

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	P60T770 w11	1.0	7B827353	P51A*472ESXA	ATP1 LQFP 144 Int-SMPS	SMPS assessment
2	P60T78 w11	1.0	7B828878	P51A*472ESXA	ATP1 LQFP 144 Int-SMPS	SMPS assessment
3	P62N51 w09	2.0	AA921086	E51A*472ESXB	ASEKH LQFP 144 Int-SMPS	SMPS assessment & Die assessment
4	P60T78 w10	1.0	7B828A9P	P1PG*472ESXA	ATP3 UFBGA 132 Legacy	Die assessment
5	P60T77 w10	1.0	7B828A9R	P1PG*472ESXA	ATP3 UFBGA 132 Legacy	Die assessment
6	P62N51 w09	2.0	7B920A6G	P1PG*472ESXB	ATP3 UFBGA 132 Legacy	Die assessment
7	P60T77 w20	1.0	AA904021	E11A*472ESXA	ASEKH LQFP 144 Legacy	Die assessment
8	P62N51 w09	2.0	AA921088	E11A*472ESXB	ASEKH LQFP 144 Legacy	Die assessment
9	P60T77 w25	1.0	7B850A7E	P2PG*472ESXA	ATP3 UFBGA 132 Ext-SMPS	Die assessment
10	P62N51 w09	2.0	7B920A7B	P2PG*472ESXB	ATP3 UFBGA 132 Ext-SMPS	Die assessment
11	P60T77 w20	1.0	AA904022	E11L*472ESXA	ASEKH LQFP 100 Legacy	Package assessment
12	P62N51 w09	2.0	AA921087	E01L*472ESXB	ASEKH LQFP 100 Int-SMPS	Package assessment
13	P62N53 w10	2.0	GQ94227R	715W*472XXXB	JSCC LQFP 64 Legacy	Package assessment
14	P62N53 w10	2.0	GQ9422A8	725W*472XXXB	JSCC LQFP 64 Int-SMPS	Package assessment
15	P62N53 w10	2.0	GQ94227P	705W*472XXXB	JSCC LQFP 64 Ext-SMPS	Package assessment
16	P62N53 w09	2.0	GQ9342AH	705B*472XXXB	JSCC LQFP 48 Legacy	Package assessment
17	P62N53 w09	2.0	GQ94229X	725B*472XXXB	JSCC LQFP 48 Ext-SMPS	Package assessment
18	P62N53 w12	2.0	GQ9422A1	70MI*472XXXB	JSCC UFQFPN 48L Legacy	Package assessment
19	P62N53 w12	2.0	GQ9422A2	72MI*472XXXB	JSCC UFQFPN 48L Ext-SMPS	Package assessment
20	P60T77 w17	1.0	A583500A	T0FY*472ESXA	ATT1 WLCSP 81L Int-SMPS	Package assessment
21	P60T77 w16	1.0	A583800K	T1FY*472ESXA	ATT1 WLCSP 81L Ext-SMPS	Package assessment
22	P62N54 w06	2.1	AA006008	E51A*472ESXZ	ATP1 LQFP 144 Int-SMPS	SMPS assessment & Die assessment
23	P62N54 w04	2.1	7B003A8M	P1PG*472ESXZ	ATP3 UFBGA 132 Legacy	Die assessment

24	P62N54 w07	2.1	AA006009	E11A*472ESXZ	ASEKH LQFP 144 Legacy	Die assessment
25	P62N54 w05	2.1	7B004A3U	P2PG*472ESXZ	ATP3 UFBGA 132 Ext-SMPS	Die assessment

3.2 Test plan and results summary

Table 5 - ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL SMPS	JESD22 A108	Ta=125°C Duration= 1200H 3V6	3	77	231	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77	Stress done on chipboard
HTOL SMPS	JESD22 A108	Ta=125°C Duration= 168H 3V6	1	77	77	Lot22 : 0/77	Stress done on chipboard
ELFR SMPS	JESD22-A108 JESD74	Ta=125°C Duration= 48H 3V6	3	500	1500	Lot1: 0/500 Lot2: 0/500 Lot3: 0/500	Stress done on chipboard
HTOL (Without SMPS)	JESD22 A108	Ta=125°C Duration= 1200H 3V6	3	77	231	Lot4: 0/77 Lot5: 0/77 Lot6: 0/77	
HTOL (Without SMPS)	JESD22 A108	Ta=125°C Duration= 168H 3V6	1	77	77	Lot 23: 0/77	
ELFR (Without SMPS)	JESD22-A108 JESD74	Ta=125°C Duration= 48H 3V6	3	500	1500	Lot4: 0/500 Lot5: 0/500 Lot6: 0/500	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	6	3	18	Lot3: 0/3 Lot8: 0/3 Lot10: 0/3 Lot22: 0/3 Lot24: 0/3 Lot25: 0/3	
LatchUp	JESD78	130°C	6	3	18	Lot3: 0/3 Lot8: 0/3 Lot10: 0/3 Lot22: 0/3 Lot24: 0/3 Lot25: 0/3	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C - Duration 1500H	3	77	231	Lot4: 0/77 Lot5: 0/77 Lot6: 0/77	
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C - Duration 168H	3	77	231	Lot4: 0/77 Lot5: 0/77 Lot6: 0/77	

EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C - Duration 168H	3	77	231	Lot4: 0/77 Lot5: 0/77 Lot6: 0/77	

Table 6 - ACCELERATED ENVIRONMENT STRESS TESTS

LQFP20x20 144L, ASE

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	5	3	15	Lot3: 0/3 Lot7: 0/3 Lot8: 0/3 Lot22: 0/3 Lot24: 0/3	

LQFP14x14 100L, ASE

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	2	3	6	Lot11: 0/3 Lot12: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot11: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot11: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H ☒ After PC	1	77	77	Lot11: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000H ☒ After PC	1	77	77	Lot11: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot11: 0/77	

LQFP10x10 64L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	3	3	9	Lot13: 0/3 Lot14: 0/3 Lot15: 0/3	

LQFP7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	2	3	6	Lot16: 0/3 Lot17: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot16: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot16: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H ☒ After PC	1	77	77	Lot16: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000H ☒ After PC	1	77	77	Lot16: 0/77	

THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot16: 0/77	

UFQFN7x7 48L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	2	3	6	Lot20: 0/3 Lot21: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot20: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot20: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96H ☒ After PC	1	77	77	Lot20: 0/77	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000H ☒ After PC	1	77	77	Lot20: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot20: 0/77	

UFBGA7X7 132L, ATP3

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	4	3	12	Lot4: 0/3 Lot9: 0/3 Lot10: 0/3 Lot25: 0/3	

WLCSP 81, ATT3

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	2	3	6	Lot20: 0/3 Lot21: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Pascal CARDOSI Muriel GALTIER	Initial release	Div. Quality Manager	Rousset	Pascal NARCHE	27-Nov-2019
			Q&R Quality Manager	Rousset	Frederic BRAVARD Dominique GALIANO	23-Oct-2019
1.1	Pascal CARDOSI Muriel GALTIER	package updates	Q&R Quality Manager	Grenoble	Dominique GALIANO	14-Feb-2020
1.2	Pascal CARDOSI Muriel GALTIER	Update with results for cut2.1qualification - PCN11971	Q&R Quality Manager	Grenoble	Dominique GALIANO	06-Apr-2020

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STM32L562QEI6	STM32L552RET6P	STM32L552QEI6Q
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STM32L562CEU6P	STM32L552ZET6Q	STM32L552QCI6Q
STM32L562CET6P	STM32L552CCT6	STM32L552CCU6
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