PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/19/11700
1.3 Title of PCN	L9945xx and ATIC235xx (UR53 silicon line): Activation of Catania 8" as additional Frond End Location beside current Agrate 8"
1.4 Product Category	see list
1.5 Issue date	2019-08-30

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Elena Maria PERNIGOTTI
2.1.2 Marketing Manager	Maurizio GALLINARI
2.1.3 Quality Manager	Marcello Donato MENCHISE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	Catania 8" and Agrate 8" Frond End Locations

4. Description of change		
	Old	New
4.1 Description	Agrate 8" Frond End Location	Catania 8" and Agrate 8" Frond End Locations
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Capacity Increase
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Codes

7. Timing / schedule	
7.1 Date of qualification results	2019-07-24
7.2 Intended start of delivery	2020-06-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description			
8.2 Qualification report and qualification results	In progress	Issue Date	

9. Attachments (additional documentations)

11700 Public product.pdf
11700 UR53_Catania_Fab transfer_Qual Plan_rev0_18-June-2019.pdf
11700 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L9945TR	

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PCN Title : L9945xx and ATIC235xx (UR53 silicon line): Activation of Catania 8" as additional Frond End Location beside current Agrate 8"

PCN Reference : ADG/19/11700

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

L9945TR		

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PRODUCT/PROCESS CHANGE NOTIFICATION

SUBJECT L9945xx and ATIC235xx (UR53 Silicon Line): Activation of Catania 8" as additional Frond End Location beside current Agrate 8"

IMPACTED PRODUCTS	ST Commercial Products involved: • L9945 • L9945TR • ATIC235 • ATIC235-TR
IMPACTED MANUFACTURING STEPS	Wafer Fab (Diffusion)
INVOLVED PLANTS	ST Catania 8” (Catania-Italy) receiving Plant ST Agrate 8” (Agrate-Italy) sending Plant
CHANGE REASON	Capacity Increase
CHANGE DESCRIPTION	Catania 8" wafer Fab will be activated as additional Front End location beside current Agrate 8"
TRACEABILITY	Dedicated Finished Good Codes ES available by W50’19 CS available by W20’20
REPORTS	Qualification report will be available within May 2020 Q100 Qualification plan: - 11700 UR53_Catania-Fab transfer Qual Plan_rev0_18-June-2019.pdf

Q100 Qualification Test Plan

Automotive Grade Level = 1 -40°C to +125°C MSL = 3

Supplier Name:	STMicroelectronics	**General Specification:**	AEC-Q100 Rev. H
Supplier Code:	UR53	**Supplier Wafer Fabrication:**	Catania
Supplier Part Number:		**Supplier Wafer Test:**	Catania
Supplier Contact:	G. Carlino / A. Tortora / M. Forestiero	**Supplier Assembly Site:**	Muar
Supplier Family Type:	BCD8SAuto Catania / TQFP64 10x10 exp pad down (Cu wires 1.2mils)	**Supplier Final Test Site:**	Muar
Device Description:		**Supplier Reliability Signature:**	G. Carlino
PPAP Submission Date:		**Customer Test ID:**	
Reason for Qualification:	Fab transfer	**Customer Part Number:**	
Prepared by Signature:	Date:18/June/2019	**Customer Approval Signature:**	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for TC, THB, AC, HTRB, PTC and HTOL; Peak Reflow Temp = 260°C	Min. MSL = 3			MSL = 3	+ 100cy after reflow
THB	A2	JESD22 A101	Temperature Humidity Bias: (Test @ Rm/Hot) 1000h, 85°C/85% R.H.	1	77	77	of	1 lot at 1000h + Family Data.
AC	A3	JESD22 A102	Autoclave: (Test @ Room) 96h, 121°C / 2 atm	1	77	77	of	1 lot at 96h + Family Data.
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) 1000cy, -55°C / +150°C	1	77	77	of	1 lot at 1000cy + Family Data.
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Room/Hot) 1000cy, Ta=-40°C / Tj = +137°C	-	-	-	-	Not required. Pd < 1W (typical condition)

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Room/Hot) 1000h, Ta=150°C	1	45	45	of	1 lot at 1000h + Family Data.

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Cold/Hot) 1236h, Tj=160°C	1	77	77	of	1 lot at 1236h@Tj=160°C + Family Data.
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot)	-	-	-	of	Family Data.
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	-	-	-	of	N/A

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts min.		All measurement within spec limits	according to AEC_Q100
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts min.		All measurement within spec limits	according to AEC_Q100
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	All measurement within spec limits	according to AEC_Q100
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	All measurement within spec limits	according to AEC_Q100
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	3	50 balls			N/A
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	1	50 leads			N/A

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Electromigration	-	-	-		Process qualification data
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown	-	-	-		Process qualification data

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
HCI	D3	JESD60 & 28	Hot Carrier Injection	-	-	-		Process qualification data
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-		Process qualification data
SM	D5	JESD61, 87, & 202	Stress Migration:	-	-	-		Process qualification data

TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test	All	All	All	of	
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)		See test method		of	1 lot
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads / Class C4B or better)		See test method		of	1 lot
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)		6		of	1 lot
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)				of	Covered by Electrical Characterization
FG	E6	AEC-Q100-007	Fault Grading: FG shall be = or > 90% for qual units	-	-	-	Fault Grade	
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-		Covered by Electrical Characterization
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	-	-	-		EMC lab
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-		NA => The device is a PRE-driver
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-		NA

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-		Covered by Test group A & C

TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Reject units outside avg.	applied in production
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	applied in production

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)

MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	-	-	-	-	NA
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	-	-	-	NA
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	-	NA
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	-	NA
DROP	G5	----------	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	-	NA
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	-	-	-	NA
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	-	-	-	NA
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	-	-	-	NA