PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/17/10607
1.3 Title of PCN	DPAK IGBT and IGBT+Diode Assembly Capacity Expansion - Tongfu Microelectronics (China)
1.4 Product Category	IGBT
1.5 Issue date	2017-12-07

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Maurizio GIUDICE
2.1.2 Marketing Manager	Anna MOTTESE
2.1.3 Quality Manager	Vincenzo MILITANO

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	New direct material part number (same supplier, different supplier or new supplier), Lead frame base material	Tongfu Microelectronics (China)

4. Description of change		
	Old	New
4.1 Description	Selected DPAK IGBTs were manufactured in Shenzhen (China)	Selected DPAK IGBTs will be manufactured also in Tongfu Microelectronics (China)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	no impact	

5. Reason / motivation for change	
5.1 Motivation	Improve service to Customers
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	by "GF" as first digits of the trace code, internal code (Finished Good) and Q.A. number

7. Timing / schedule	
7.1 Date of qualification results	2017-12-04
7.2 Intended start of delivery	2018-03-11
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	10607 Rel07-17.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2017-12-07

9. Attachments (additional documentations)

10607 Public product.pdf
10607 DPAK IGBT and IGBT+Diode Assembly Capacity Expansion - TFME.pdf
10607 Rel07-17.pdf
10607 Comparison.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STGD14NC60KT4	
	STGD4M65DF2	
	STGD5H60DF	
STGD5NB120SZT4	STGD5NB120SZT4	
	STGD6M65DF2	
	STGD6NC60HDT4	
STGD7NB60ST4	STGD7NB60ST4	
STGD7NC60HT4	STGD7NC60HT4	

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Reliability Report Plan

DPAK IGBT and IGBT+Diode Assembly Capacity Expansion
in Tongfu Microelectronics (China)
INDUSTRIAL

General Information	
Product Lines:	IGBT EI6201 - Diode F62B IGBT IV6201 - Diode F62I IGBT IV6401
P/N:	STGD5H60DFSF STGD6NC60HDT4 STGD7NC60HT4
Product Group:	ADG
Product division:	Power Transistor Division
Package:	DPAK
Silicon Process techn.:	IGBT Planar IGBT Trench

Locations	
Wafer Fab and EWS Plant:	*IGBT: Catania (Italy)* *Diode:Tours (France)*
Assembly and testing plant:	*Tongfu Microelectronics (China)*
Reliability Lab:	*ADG - Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	November 2017	8	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify DPAK IGBT and IGBT+Diode assembled in TONGFU Microelectronics (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

IGBT Planar / IGBT Trench

4.2 Construction note

D.U.T.: STGD5H60DFSF PACKAGE: DPAK

Wafer/Die Information	
Technology	IGBT Trench - Diode
Wafer Fab	IGBT Catania (Italy) - Diode *Tours (France)*
Die finishing back side	IGBT Al/Ti/NiV/Ag
Die size	IGBT: 2510 x 1950 µm^2 / Diode: 1100 x 1100 µm^2
Metal	IGBT AlCu
Passivation type	GBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (15mils)
Lead finishing/bump solder material	Pure Tin

D.U.T.: STGD6NC60HDT4 PACKAGE: DPAK

Wafer/Die Information	
Technology	IGBT Planar - Diode
Wafer Fab	IGBT Catania (Italy) - Diode *Tours (France)*
Die finishing back side	IGBT Cr/Ni/Ag
Die size	IGBT 1690 x 2620 µm^2 / Diode: 1100 x 1100 µm^2
Metal	IGBT AlSi
Passivation type	IGBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (5mils)
Lead finishing/bump solder material	Pure Tin

D.U.T.: STGD7NC60HT4 **PACKAGE: DPAK**

Wafer/Die Information	
Technology	IGBT Planar
Wafer Fab	IGBT Catania (Italy)
Die finishing back side	IGBT Cr/Ni/Ag
Die size	IGBT 3500 x 2880 µm^2
Metal	IGBT AlSi
Passivation type	IGBT SiN (nitride)

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Soft Solder UMICORE Pb/Sn/Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Al (5mils) Source: Al (10mils)
Lead finishing/bump solder material	Pure Tin

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot	Part Number	Silicon Lines	Package	Wafer Fab	Assy Plant	Comments
1	STGD5H60DFSF	EI62	DPAK	Catania (Italy)	Tongfu Microelectronics (China)	
2	STGD6NC60HDT4	IV62				
3	STGD7NC60HT4	IV64				

5.2 Reliability test plan summary

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/190	0/190	0/190
2	**External visual**		JESD22 B-101	All devices submitted for testing			0/190	0/190	0/190
Silicon Oriented Test									
3	**HTRB**	N	JESD22 A-108	Tj = 150°C ; BIAS = 480V	45 x lot	1000H	04/2018	04/2018	04/2018
4	**HTGB**	N	JESD22 A-108	Tj=150°C ; BIAS= 25V	45 x lot	1000H	04/2018	04/2018	04/2018
Package Oriented Test									
5	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times	All devices to be subjected to H3TRB, TC, AC	Final	04/2018	04/2018	04/2018
6	**TC**	Y	JESD22 A-104	TA=-65°C TO 150°C 1 HOURS / CYCLE	25 x lot	500cy	04/2018	04/2018	04/2018
7	**AC**	Y	JESD22 A-102	TA=121°C ; PA=2ATM	25 x lot	96H	04/2018	04/2018	04/2018

8	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=80V	25 x lot	1000H	04/2018	04/2018	04/2018
9	**IOL**	N	MIL-STD-750 Method 1037	ΔTj ≥105°C	25 x lot	10Kcy	04/2018	04/2018	04/2018
10	**ESD**		ESDA-JEDEC_ JES-001 ANSI-ESD S5.3.1	CDM / HBM	3 x lot		04/2018	04/2018	04/2018
11	**Physical Dimension**		JESD22 B-100		30 x lot		0/30	0/30	0/30
12	**Solderability**		J-STD-002		10 x lot		0/10	0/10	0/10
13	**Terminal Strength**		MIL-STD-750 Method 2036		30		0/30	0/30	0/30
14	**Bond Shear**		JESD22 B-116		10 bonds from min of 5 devices		0/5	0/5	0/5
15	**Resistance to Solder Heat**		JESD22 A-111		12		0/12	0/12	0/12

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB / HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
IOL / TF Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.