# PRODUCT / PROCESS CHANGE NOTIFICATION

| 1. PCN basic data | |
|---|---|
| 1.1 Company | STMicroelectronics International N.V |
| 1.2 PCN No. | ADG/17/10582 |
| 1.3 Title of PCN | Wafer Thickness Reduction for STL70N4LLF5 and STL15DN4F5 produced in Catania Front End Site |
| 1.4 Product Category | Power MOSFET |
| 1.5 Issue date | 2017-11-24 |

| 2. PCN Team | |
|---|---|
| 2.1 Contact supplier | |
| 2.1.1 Name | ROBERTSON HEATHER |
| 2.1.2 Phone | +1 8475853058 |
| 2.1.3 Email | heather.robertson@st.com |
| 2.2 Change responsibility | |
| 2.2.1 Product Manager | Riccardo NICOLOSO |
| 2.1.2 Marketing Manager | Antonino PELLEGRINO |
| 2.1.3 Quality Manager | Vincenzo MILITANO |

| 3. Change | | |
|---|---|---|
| 3.1 Category | 3.2 Type of change | 3.3 Manufacturing Location |
| Wafer Fab (Process) | Backside finish modification except for wafer for sale: change in deposition material type/nature/thickness | Catania Front end |

| 4. Description of change | | |
|---|---|---|
| | Old | New |
| 4.1 Description | Back Side Grinding before metalization down to Final Wafer thickness = 200µm | Back Side Grinding before metalization down to Final Wafer Thickness = 70µm |
| 4.2 Anticipated Impact on form,fit, function, quality, reliability or processability? | No Impact in terms of electrical, physical and functional aspects | |

| 5. Reason / motivation for change | |
|---|---|
| 5.1 Motivation | Wafer thickness range rationalizatio on silicon lines assembled in PowerFLATTM with the target to optimize the process, materials usage and availability. |
| 5.2 Customer Benefit | SERVICE IMPROVEMENT |

| 6. Marking of parts / traceability of change | |
|---|---|
| 6.1 Description | by FG code and Q.A. number |

| 7. Timing / schedule | |
|---|---|
| 7.1 Date of qualification results | 2018-03-18 |
| 7.2 Intended start of delivery | 2018-04-08 |
| 7.3 Qualification sample available? | Upon Request |

| 8. Qualification / Validation | | | |
|---|---|---|---|
| 8.1 Description | | | |
| 8.2 Qualification report and qualification results | In progress | Issue Date | |

| 9. Attachments (additional documentations) |
|---|
| 10582 Public product.pdf<br>10582 PCN - Wafer Thickness Reduction for STL70N4LLF5 and STL15DN4F5 produced ....doc |

| 10. Affected parts | | |
|---|---|---|
| 10. 1 Current | | 10.2 New (if applicable) |
| 10.1.1 Customer Part No | 10.1.2 Supplier Part No | 10.1.2 Supplier Part No |
| | STL15DN4F5 | |
| | STL70N4LLF5 | |

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Automotive Discrete Group (ADG)
Power Transistor Division

# Process Change Notification

## Wafer Thickness Reduction for STL70N4LLF5 and STL15DN4F5 produced in Catania Front End Site

Dear Customer,

Based on our continuous improvement policy and according to the rationalization plan currently running on our product portfolio, we are pleased to inform you that we are introducing a reduction on wafer thickness for products STL70N4LLF5 and STL15DN4F5 produced in Catania Front End site. The products are both assembled in our Shenzhen (China) back end in PowerFLAT™ package.

The change has been classified as Class 1 according to ZVEI and ST internal rules.

| | **Assessment of impact on Supply Chain regarding following aspects**<br>- contractual agreements<br>- technical interface of processability/manufacturability of customer<br>- form, fit, function, quality performance, reliability | **Remaining risks on Supply Chain?** | |
|---|---|---|---|
| **ID** | **Type of change** | **No** | **Yes** |
| SEM-PW-03 | New final wafer thickness | **P** | **P** |

In the following pages we are reporting a detailed analysis of the change.
The plan to complete the qualification is the following:

- Assembly Workability
- Reliability Assessment

Final Release by week 10/2018.

Sincerely Yours!

## Wafer Thickness Reduction for STL70N4LLF5 and STL15DN4F5 produced in Catania Front End Site

**ST Part number:**

ST PN: **STL70N4LLF5 / STL15DN4F5**
Front End plant: **Catania M5**
Package: **PowerFLAT™**
Back End plant: **Shenzhen**

**Reason and background of the change**

To rationalize the wafer thickness range on silicon lines assembled in PowerFLAT™ with the target to optimize the process, materials usage and availability.

**Detailed description of change(s), including affected type of changes**

Final Wafer thickness from (current) 200µm down to (new) 70µm

| Old Process | New Process |
|---|---|
| • Back Side Grinding<br>o Wafer Thickness = 200µm<br>• Back Side Metal | • Back Side Grinding<br>o Wafer Thickness = 70µm<br>• Back Side Metal |

**Evaluation performed on Test Vehicle: STL70N4LLF5**

The reduction wafer thickness will have two effects:

- On-Resistance ($R_{DSon}$) reduction
- Thermal Resistance ($R_{TH}$) reduction → improvement on product thermal behaviour

Here below the outcome of the performed analysis:

**$R_{DSon}$ @ 10V / 9A (mΩ) (Samples Size > 5000pcs)**

| Item | Old Process | New Process | Delta |
|---|---|---|---|
| **Avg** | 6.44 | 6.03 | -6.1% |
| **Stdev** | 0.15 | 0.15 | 0 |
| **@ 3*Sigma** | 6.89 | 6.48 | -5.9% |

**$R_{TH\ j\text{-}case}$ (°C/W) (Sample Size 10pcs / Trial)**

| Item | Old Process | New Process | Delta |
|---|---|---|---|
| **Avg** | 1.60 | 1.35 | -15.0% |
| **Stdev** | 0.12 | 0.12 | 0 |
| **@ 3*Sigma** | 1.96 | 1.61 | -13.0% |

**Note:** The same conclusion can be extended to STL15DN4F5

**Impact on form, fit, function, or reliability.**

No Change

**Datasheet**

No Change

**Benefit of the change**

1. Increased Throughput due to material usage and process optimization
2. Improvement on On-Resistance value → better margin versus specification
3. Improvement on thermal behavior
4. Improvement on service to customer according point 1 and 2.

<table>
<tr><td>Planned Implementation date for change</td><td>Qualification on going according to the plan reported at point below.</td></tr>
<tr><td>Comparative analysis</td><td>Except the $R_{DSon}$ and $R_{TH}$, No impact on the other electrical static and dynamic parameters</td></tr>
<tr><td>Qualification Plan</td><td>The qualification plan, elaborated according AEC-Q101, is the following:<br><br>Test Vehicle: STD70N4LLF7<br>Silicon Line: 5H4C<br><br>
<table>
<tr><th>Item</th><th>Description</th><th>Status</th><th>Sample Size</th></tr>
<tr><td>Workability</td><td>Workability assessment during assembly<br>• Wire Bond Strength<br>• Wire Bond Shear</td><td>Done</td><td>3 Lots</td></tr>
<tr><td>PV</td><td>Parametric Verification at Final Testing</td><td>Done</td><td>3 Lots</td></tr>
<tr><td>HTRB</td><td>High Temperature Reverse Biased</td><td>Wk 10/2018</td><td>77pcs / 3 Lots</td></tr>
<tr><td>TC</td><td>Thermal Cycle</td><td>Wk 10/2018</td><td>77pcs / 3 Lots</td></tr>
<tr><td>IOL</td><td>Intermittent Operative Life</td><td>Wk 10/2018</td><td>77pcs / 3 Lots</td></tr>
<tr><td>Rth</td><td>Thermal Resistence</td><td>Done</td><td>10pcs / 3 Lots</td></tr>
<tr><td>Rsh</td><td>Resistence to Solder Heat</td><td>Wk 10/2018</td><td>30pcs / 3 Lots</td></tr>
</table>
<br>Proposed Implementation Date → week 13/2018</td></tr>
<tr><td>PPAP Update</td><td>To be applied after official customer acceptance</td></tr>
</table>