PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMG/17/10438
1.3 Title of PCN	Qualification of ST Ang Mo Kio (Singapore) as wafer fab for VIPOWER M0K5 products
1.4 Product Category	All products with VIPOWER M0K5 (see attached list)
1.5 Issue date	2017-11-10

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Lorenzo NASO
2.1.2 Marketing Manager	Marcello SAN BIAGIO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer of a full process or process brick (process step, control plan, recipes) from one site to another site	Wafer fabrication site	Catania CT6, Ang Mo Kio AMK6

4. Description of change		
	Old	New
4.1 Description	Wafer fab for VIPOWER M0K5 : ST Catania (Italy)	Wafer fab for VIPOWER M0K5 : ST Ang Mo Kio (Singapore). VIPOWER by M0K5 technology will be not manufactured in Catania Wafer fab from H2'2018.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	ST Ang Mo Kio will be validated as an additional wafer fab for VIPOWER M0K5 products in order to provide more flexibility in term of production and prepare the termination of the production of these products in ST Catania (Italy).
5.2 Customer Benefit	MANUFACTURING FLEXIBILITY

6. Marking of parts / traceability of change	
6.1 Description	New dedicated genealogy

7. Timing / schedule	
7.1 Date of qualification results	2017-10-30
7.2 Intended start of delivery	2018-02-15
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	10438 251-W-17-STEF01FTR+STEF12WPUR.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2017-11-10

9. Attachments (additional documentations)
10438 Public product.pdf 10438 251-W-17-STEF01FTR+STEF12WPUR.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STEF12EPUR	
	STEF12PUR	
	STEF12WPUR	

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Reliability Evaluation Result

New Product Evaluation

STEF01FTR
+
M0K5 technology transfer from CT6 to AMK6

T.Vs.: STEF12WPUR
STEF01FTR

General Information	
Product Lines	UAX001
Product Description	Fully programmable Universal Electronic fuse
P/N	*STEF01FTR*
Product Group	*AMG*
Product division	*GENERAL PURPOSE ANALOG & RF*
Package	HTSSOP 14 4.4 PITCH 0.65 EXPAD *Stacked die*
Silicon Process technology	*Controller BCD8sp (DIE 1) (VNZ9, VIPower M0K5 (DIE 2)*

Locations	
Wafer fab	*AGRATE AG8+R2 (DIE 1)* *CATANIA CTM6 (DIE 2) Lot 1* *AMK (DIE 2) Lot 2-3*
Assembly plant	UTAC Thai Limited
Reliability Lab	*Catania Reliability LAB*
Reliability assessment	*Pass*

General Information	
Product Lines	UC3001
Product Description	
P/N	*STEF12WPUR*
Product Group	*AMG*
Product division	*GENERAL PURPOSE ANALOG & RF*
Package	VDFPN 3x3x1.0 10 PITCH 0.50
Silicon Process technology	*Controller BCD3S (DIE 1) (VNX1, VIPower M0K5 (DIE 2)*

Locations	
Wafer fab	*AMK (DIE 1)* *AMK (DIE 2)*
Assembly plant	CARSEM China
Reliability Lab	*Catania Reliability LAB*
Reliability assessment	*See conclusion*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	June-2017	6	Giuseppe Giacopello	Giovanni Presti	*REL. 6088.144-W-17 Final Report on STEF01FTR*
2	August-2017	7			*REL. 6088.251-W-17 Final Report including STEF12WPUR*

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

- **AIM 1:** To qualify the New Product STEF01FTR on HTSSOP 14 4.4 PITCH 0.65 EXPAD package with stacked die.

    1. Die 1: BCD8sp Controller
    2. Die 2: M0K5 Viper

    HTSSOP 14 4.4 PITCH 0.65 EXPAD, Stacked die UTAC

- **AIM 2:** To validate the M0K5 technology transfer from CT6 to AMK6

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime

4 DEVICE CHARACTERISTICS

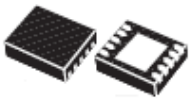
4.1 Device description

Description

TSSOP14
Exposed pad
(HTSSOP14)

The STEF01 is an universal integrated electronic fuse optimized for monitoring the output current and the input voltage, over the DC power lines.
When connected in series to the main power rail, it is able to detect and react to over-current and over-voltage conditions. When an over load condition occurs the device limits the output current to a safe value defined by the user. If the anomalous overload condition persists it goes to the open state, disconnecting the load from the power supply.
The device is fully programmable: UVLO ,overvoltage clamp and startup time can be set by means of external components.
The programmable turn-on time is useful to keep under control the in-rush current during startup and hot-swap operations. The device is able to operate in thermal latch and auto-retry protection modes, which are selectable by means of a dedicated pin.
The STEF01 provides a gate driver pin that can be used to turn-off an external power MOSFET, implementing a reverse current blocking circuit.
The intervention of the thermal protection is signalled to the board monitoring circuits through an appropriate signal on the Fault pin.

Description



DFN10 (3x3 mm)

The STEF12 is an integrated electronic fuse optimized for monitoring output current and input voltage. Connected in series to a 12 V rail, it is capable of protecting the electronic circuitry on its output from overcurrent and overvoltage. The device has a controlled delay and turn-on time. When an overload condition occurs, the STEF12 limits the output current to a predefined safe value. If the anomalous overload condition persists it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when power is re-applied the E-fuse initially limits the output current to a safe value and then again goes into an open state. The device is equipped with a thermal protection circuit. The intervention of the thermal protection is signalled to the board monitoring circuits through a signal on the Fault pin. Unlike the mechanical fuses, which must be physically replaced after a single event, the Efuse does not degrade in its performance after short-circuit/thermal protection interventions and it is reset either by recycling the supply voltage or using the Enable pin. The companion chip for the 5 V power rails is also available with part number STEF05.

4.2 Construction note

	P/N: *STEF01FTR*				P/N: *STEF12WPUR*	
Wafer/Die fab. information	**1st Lot (Intermediate process)**		**2nd Lot and 3rd Lot (Final Process)**		**4th Lot (Final Process)**	
	DIE 1 (UAX0)	**DIE 2 (VNZ9)**	**DIE 1 (UAX0)**	**DIE 2 (VNZ9)**	**DIE 1 (UC30)**	**DIE 2 (VNX1)**
Wafer fab manufacturing location	AGRATE AG8+R2	Catania CTM6	AGRATE AG8+R2	Singapore 6	Singapore 6	Singapore 6
Technology	BCD8sP	VIPower M05	BCD8sP	VIPower M05	BCD 3 - 3S	VIPOWER M05
Process Family	BCD8SP 4m	VIPOWER M0K5	BCD8SP 4m	VIPOWER M0K5	BCD3S	VIPower M0K5
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	Ti-Ni-Au
Die size	1606 x 1606 micron	2265 x 2827 micron	1606 x 1606 micron	2265 x 2827 micron	1700 x 1140 micron	1590 x 890 micron
Wafer Testing (EWS) information						
Electrical testing manufacturing location	Ang Mo Kio EWS				Ang Mo Kio EWS	
Tester	asl1k				ETS364	
Test program	UAX0_0220.nx4					
Assembly information						
Assembly site	UTAC Thai Limited				CARSEM China	
Package description	HTSSOP 14 4.4 PITCH 0.65 EXPAD				VDFPN 3x3x1.0 10 PITCH 0.50	
Molding Compound	EPOXY				EPOXY	
Frame Material	P/N FI0144 14L ETSSOP 142x126, Selective Ag				P/N #442655 DFN 3X3 10L 104X75 RT-PPF	
Die Attach Material	EPOXY				EPOXY	
Wires Bonding Mat.	1.3 mils Cu wire and 2.0 mils Cu wire				gold wires of 2mils	
Final testing information						
Testing location	UTAC Thai Limited				CARSEM China	
Tester	ASL1K				ASL1K	
Test program	STEF01_FT_UTAC_0210.nx4				STEF12_REV_6_1_SINGLE_BIN	

4.3 Test vehicle

Lot #	Process/ Package	Product Line
1	Die 1: BCD8sp Controller Die 2: M0K5 Viper HTSSOP 14 4.4 PITCH 0.65 EXPAD	STEF01FTR UAX0
2		
3		
4	Die 1: BCD3S Controller Die 2: M0K5 Viper VDFPN 3x3x1.0 10 PITCH 0.50	STEF12WPUR - UC30

5 TEST PLEVALUATION PLAN AND RESULTS SUMMARY

P/N:

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1 STEF01	**Lot 2 STEF01**	**Lot 3 STEF01**	**Lot 4 STEF12**	
Die Oriented Tests										
HTOL	N	JESD22 A-108	**Tj = 125° C, BIAS= 7 V; 55 V** (STEF01FTR) **BIAS= 18 V** (STEF12WPUR)		168 h	**0/77**	**0/77**	**0/77**	**0/77**	
					500 h	**0/77**	**0/77**	**0/77**	**0/77**	
					1000 h	**0/77**	**0/77**	**0/77**	**0/77**	
HTSL	N	JESD22 A-103	**Ta = 150° C**		168 h	**0/25**	**0/25**	**0/25**	**0/25**	
					500 h	**0/25**	**0/25**	**0/25**	**0/25**	
					1000 h	**0/25**	**0/25**	**0/25**	**0/25**	
HTSL	N	JESD22 A-103	**Ta = 175° C**		168 h	**0/25**	**0/25**	**0/25**	**-**	Engineering evaluation
					500 h	**0/25**	**0/25**	**0/25**	**-**	
					1000 h	**0/25**	**0/25**	**0/25**	**-**	
Package Oriented Tests										
PC		JESD22 A-113	**Drying 24 H @ 125° C Store 40h @ Ta= 60° C Rh= 60% Over Reflow @ Tpeak=260° C 3 times**		Final	**Pass**	**Pass**	**Pass**	**-**	
AC	Y	JESD22A-102	**Pa= 2Atm / Ta= 121° C**		96h	**0/25**	**0/25**	**0/25**	**0/25**	
					168h	**0/25**	**0/25**	**0/25**	**0/25**	Engineering evaluation
TC	Y	JESD22 A-104	**Ta = -65° C to 150° C**		100 cy	**0/25**	**0/25**	**0/25**	**0/25**	
					200 cy	**0/25**	**0/25**	**0/25**	**0/25**	
					500 cy	**0/25**	**0/25**	**0/25**	**0/25**	
THB	Y	JESD22 A-101	**Ta = 85° C, RH = 85%, BIAS= 5.6 V; 44 V**		168 h	**0/25**	**0/25**	**0/25**	**0/25**	
					500 h	**0/25**	**0/25**	**0/25**	**0/25**	
					1000 h	**0/25**	**0/25**	**0/25**	**0/25**	
Other Tests										
ESD	N	ANSI/ESDA/JEDEC JS001	**HBM**	3	±2KV	-	-	**Pass**	-	**Report 305_2016_ UAX0ACA - STEF01**
		ANSI/ESDA/JEDEC JS002	**CDM**	3	±500V	-	-	**Pass**	-	
LU	N	JESD78x	**Current Inj. Overvoltage**	9	±200mA	-	-	**Pass**	-	

Note : All The samples will be assembled on chip boards according to *IPC /JEDEC J-STD 020D*

5.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model **HBM**: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.