PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/20/10426
1.3 Title of PCN	Product Change Notification on selected BlueNRG-2 products
1.4 Product Category	BlueNRG-2 products
1.5 Issue date	2020-04-14

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Marco VENERI
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	Diffusion plant : TSMC Taiwan

4. Description of change		
	Old	New
4.1 Description	Current version	1) Register DIE_ID now return 0x112. 2) Extended BOR operating voltage down to 1.7V 3) Fix on SWD interface. 4) Minor functional fixes on AUXADC. 5) Extended packet length supported also in test-mode. 6) Other minor changes to improve the ST manufacturing FT yield. 7) Modification of datasheet and erratasheet. 8) SDK compatibility matrix updated in the SDK release Notes.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	It is recommended to use SDK 3.0.0 (June 2018) or above for proper operation. Failure to do so would result in BOR to not be enabled upon the initialization phase. No other impact on form, fit, function, reliability or processability.	

5. Reason / motivation for change	
5.1 Motivation	Following Divisional commitment towards continuous improvement, the existing BlueNRG-2 design has been improved to enhance the features and/or performance to improve ST manufacturing FT yield.
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Finish Good change, date-code and DIE_ID register value.

7. Timing / schedule	
7.1 Date of qualification results	2020-04-14
7.2 Intended start of delivery	2020-07-26
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	10426 BlueNRG1 and BLUENRG2 ReliabilityEvaluationReport_.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2020-04-14

9. Attachments (additional documentations)
10426 Public product.pdf 10426 BlueNRG1 and BLUENRG2 ReliabilityEvaluationReport_.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	BLUENRG-232	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Product Change Notification on selected BlueNRG-2 products

PCN Reference : AMS/20/10426

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

BLUENRG-232		

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Reliability Evaluation Report

Standard Consumer Grade Qualification

F128 BLUENRGQTR
F157 BLUENRG-134
F157 BLUENRG-132
F174-BLUENRG-232
F174-BLUENRG-248

General Information	
Product Line	*F157, F128,F174*
Product Description	Bluetooth Low Energy Wireless Processor
P/N	*BLUENRG-134* *BLUENRG-234* *BLUENRGQTR* *BLUENRG-232* *BLUENRG-248*
Product Group	*AMG*
Product division	*General purpose analog*
Package	*VFQFPN 5x5x0.9 32L-*
Silicon Process technology	*C090LP+flash*

Locations	
Wafer fab	*TSMC Fab14*
Assembly plant	*SUBCO ATP3, UTAC Thai*
Reliability Lab	*Grenoble GRAL*
Reliability assessment	***Pass***

PRODUCTS LIST

Product line	P/N	Package	Assy Plant
F128	BLUENRGQTR BLUENRG-MSQTR	VFQFPN 5x5 32L	SUBCO ATP3
	BLUENRGCSP BLUENRG-MSCSP	Wafer level CSP	Subco ATT1
F157	BLUENRG-134 BLUENRG-132	Wafer level CSP VFQFPN 5x5 32L	Subco ATT UTAC Thai
F174	*BLUENRG-232* *BLUENRG-234* *BLUENRG-248*	VFQFPN 5x5 32L Wafer level CSP VFQFPN 6x6 48L	Subco ATT UTAC Thai UTAC Thai

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
ADCS0061692	Reliability Tests and Criteria for Product Qualification

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The Aim of this report is to present reliability trials performed on F128 BlueNRG (MSQTR and MSCSP), F174 BlueNRG (232/234) and F157 BlueNRG (132/134) products in order to reach qualification. BlueNRG is a Bluetooth Low Energy Wireless Processor based on ARM Cortex M0 core.

3.2 Conclusion

Reliability trials have been performed with good results on both versions. Neither functional nor parametric rejects were generated by HTOL1000h and the drift analysis on 78 parts did not reveal any suspect behavior. ELFR did not reveal any extrinsic reliability issue. Package oriented tests are conclusive and no delamination was discovered. ESD & Latch-Up are in accordance with ST specs.

F128 BlueNRG, F174 BlueNRG (232/234/248) and F157 BlueNRG-134 and BlueNRG-132 products are qualified.

4 DEVICE CHARACTERISTICS

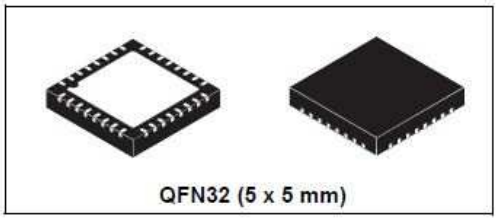
4.1 Device description

life.augmented

BlueNRG

Bluetooth® low energy wireless network processor

Datasheet - preliminary data



QFN32 (5 x 5 mm)

Features

- Bluetooth specification v4.0 compliant master and slave single-mode Bluetooth low energy network processor
- Embedded Bluetooth low energy protocol stack: GAP, GATT, SM, L2CAP, LL, RF-PHY
- Bluetooth low energy profiles provided separately
- Operating supply voltage: from 2.0 to 3.6 V
- 8.2 mA maximum TX current (@0 dBm, 3.0 V)
- Down to 1.7 µA current consumption with active BLE stack
- Integrated linear regulator and DC-DC step-down converter
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- Integrated general-purpose ADC
- Proprietary application controller interface (ACI), SPI based, allows interfacing with an external host application microcontroller
- Full link controller and host security
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- On-chip non-volatile Flash memory
- AES security co-processor
- Low power modes
- 16 or 32 MHz crystal oscillator
- 12 MHz ring oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Battery voltage monitor and temperature sensor
- Compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, ARIB STD-T66
- Available in QFN32 (5 x 5 mm) package
- Operating temperature range: -40 °C to 85 °C

Applications

- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Home and Industrial automation
- Assisted living
- Mobile phone peripherals
- PC peripherals

Table 1. Device summary

Order code	Package	Packing
BLUENRGQTR	QFN32	Tape and reel

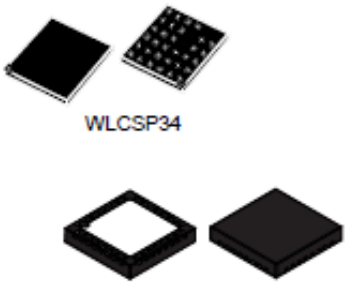
August 2013 DocID025108 Rev 1 1/34

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice. www.st.com

BlueNRG-1

Bluetooth® low energy wireless system-on-chip

Datasheet - production data



Features

- Bluetooth specification compliant master, slave and multiple roles simultaneously, single-mode Bluetooth low energy system-on-chip
- Operating supply voltage: from 1.7 to 3.6 V
- Integrated linear regulator and DC-DC step-down converter
- Operating temperature range: -40 °C to 105 °C
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- Programmable 160 KB Flash
- 24 KB RAM with retention (two 12 KB banks)
- 1 x UART interface
- 1 x SPI interface
- 2 x I²C interface
- 14 or 15 GPIO
- 2 x multifunction timer
- 10-bit ADC
- Watchdog & RTC
- DMA controller
- PDM stream processor
- 16 or 32 MHz crystal oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Battery voltage monitor and temperature sensor
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- 8.2 mA maximum TX current (@ 0 dBm, 3.0 V)
- Down to 1 µA current consumption with active BLE stack (sleep mode)
- Compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, ARIB STD-T66
- Pre-programmed bootloader via UART
- QFN32, WCSP34 package option
- Dedicated wettable flank QFN package for automotive grade qualification

Applications

- Automotive product
- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Home and industrial automation
- Assisted living
- Mobile phone peripherals
- Lighting
- PC peripherals

Table 1: Device summary table

Order code	Package	Packing
BLUENRG-132	QFN32 (5 x 5 mm)	Tape and reel
BLUENRG-134	WLCSP34	Tape and reel
BLUENRG-132Y	QFN32 (5 x 5 mm) Automotive grade Level	Tape and reel

BlueNRG-2

Datasheet

Bluetooth® low energy wireless system-on-chip

Product status link
BlueNRG-2

Features

- Bluetooth low energy single mode system-on-chip compliant with Bluetooth 5.0 specifications:
  - master, slave and multiple simultaneous roles
  - LE data packet length extension
- Operating supply voltage: from 1.7 to 3.6 V
- Integrated linear regulator and DC-DC step-down converter
- Operating temperature range: -40 °C to 105 °C
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- Programmable 256 kB Flash
- 24 kB RAM with retention (two 12 kB banks)
- 1 x UART interface
- 1 x SPI interface
- 2 x I²C interface
- 14, 15 or 26 GPIOs
- 2 x multifunction timer
- 10-bit ADC
- Watchdog and RTC
- DMA controller
- PDM stream processor
- 16 or 32 MHz crystal oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Battery voltage and temperature sensors
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- 8.3 mA TX current (@ -2 dBm, 3.0 V)
- Down to 1 µA current consumption with active BLE stack (sleep mode)
- ST companion integrated balun/filter chips are available
- Average advertisement current consumption 15.34 µA (advertisement interval 1000 ms) – 1 year, 8 months, 19 days with 230 mAh battery (CR2032)
- Average connection current consumption 7.059 µA (connection interval 1000 ms) – 3 years, 10 months, 12 days with 230 mAh battery (CR2032)
- Suitable for building applications compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 part 15, ARIB STD-T66
- Pre-programmed bootloader via UART
- QFN32, QFN48 and WCSP34 package options

Applications

- Watches

4.2 Construction note

Line:	F128 BLUENRG 1mil	F128 BLUENRG 0.8mil	F128 BLUENRG CSP	F157 BLUENRG-132	F157 BLUENRG-134	F174 BLUENRG-232	F174 BLUENRG-234
Comm. Product:	**BLUENRGQTR**	**BLUENRGQTR**	**BLUENRG CSP**	**BLUENRG-132**	**BLUENRG-134**	**BLUENRG-232**	**BLUENRG-234**
Package Type:	VFQFPN 5.0x5.0x0.9 32L-	VFQFPN 5.0x5.0x0.9 32L-	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4
Die Size:	2600 x 2500 µm	2600 x 2500 µm	2660 x 2560 µm	2710 x 2580 µm	2710 x 2580 µm	2710 x 2580 µm	2710 x 2580 µm
Diffusion Plant:	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14	TSMC Fab14
Assembly Site:	SUBCO ATP3	SUBCO ATP3	SUBCO ATT1	UTAC Thai	SUBCO ATT1	UTAC Thai	SUBCO ATT1
Test Site:	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE	GRENOBLE
Fab Process:	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash	CMOS90LP+Flash
Passivation:	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE	PSG + NITRIDE
Die backside:	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die Attach:	Ablestick AMK-6	Ablestick AMK-6	NA	Henkel 8600	NA	Henkel 8600	NA
Mold Compound:	Sumitomo G700	Sumitomo G700	NA	SUMITOMO G700	NA	SUMITOMO G700	NA
Lead Frame:	Copper	Copper	NA	Copper	NA	Copper	NA
Lead Finish:	NiPdAu	NiPdAu	Bump leadfree	Sn	Bump leadfree	Sn	Bump leadfree
Package Size and Pitch:	VFQFPN 5.0x5.0x0.9 32L-Ep0.5	VFQFPN 5.0x5.0x0.9 32L-Ep0.5	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4	VFQFPN 5X5X1.0 32L	Wafer level CSP pitch0.4
Bond Wire:	Gold 1MIL	Gold 0.8MIL	NA	Gold 0.8MIL	NA	Gold 0.8MIL	NA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	QFN32 5x5 1mil	F128	BLUENRG
2	QFN32 5x5 1mil	F128	BLUENRG
3	QFN32 5x5 0.8mil	F128	BLUENRG
4	WLCSP pitch 0.4mm	F128	BLUENRG
5	WLCSP pitch 0.4mm	F128	BLUENRG
6	QFN32 5x5 0.8mil	F157	BLUENRG1
7	WLCSP pitch 0.4mm	F174	BLUENRG2
8	QFN32 5x5 0.8mil	F174	BLUENRG2

Detailed results in below chapter will refer to Lot #.

5.2 Test plan and results summary

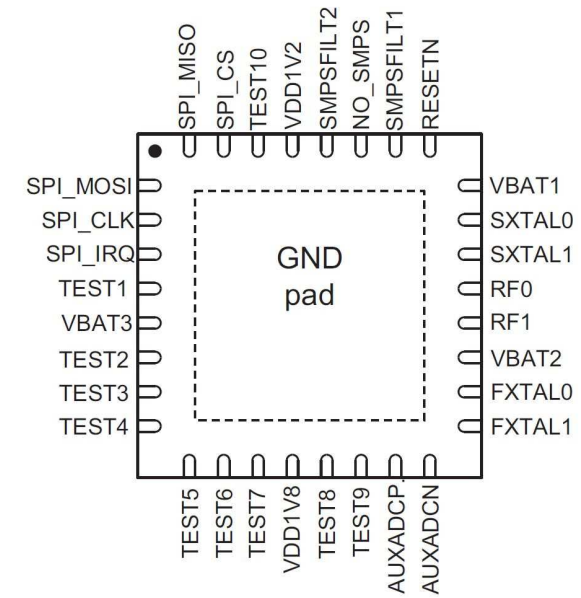
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS								Note
						Lot 1	Lot 2	Lot 3	Lot4	Lot5	Lot6	Lot7	Lot8	
Die Oriented Tests														
HTOL	N	JESD22 A-108	Tj = 125°C, BIAS		168H	0/74	0/78	0/73			0/95			
					500H	0/73	0/78	0/73			0/95			
					1000H	0/73	0/78	0/73						
HTSL	N	JESD22 A-103	Ta = 150°C		168H	0/80	-	-	0/78	0/78	-			
					500H	0/80	-	-	0/78	0/78	-			
					1000H	0/80	-	-	0/78	0/78	-			
ELFR	N	JESD74	Tj = 125°C, BIAS			-	-	0/480	0/239		-			
Package Oriented Tests														
PC		JESD22 A-113	MSL3: Bake 24H @ 125°C Soak 192H @ Ta=30°C RH=60% Oven Reflow @ Tpeak=260°C, 3 times		Final	Pass	-	Pass	Pass	Pass	-			
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96H	-	-	*0/80	*0/79	*0/80	-			*UHAST
					168H	0/78	-				-			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy	-	-	0/80	0/70	0/76	-			
					500cy	0/78	-	0/80	0/70	0/76	-			
					1000cy	0/78	-	0/80	0/70	0/76	-			
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168H	0/76	-	-			-			
					500H	0/75	-	-			-			
					1000H	0/75	-	-			-			
Other Tests														
ESD	N	ADCS 0060102 (JESD22-A114)	HBM			±3KV	-	-	Pass	-		2kV	2kV	
		ADCS 0060102 (ANSI/ESD STM5.3.1)	CDM			±1.5KV	-	-	400V			1000V	1000V	
		ADCS 0060102 (JESD22-A115)	MM			±300V	-	-	160V					
LU	N	ADCS 0018695	Current Inj. Overvoltage		±200mA X1.5	Pass	-	-	Pass			Pass	Pass	

6 ANNEXES

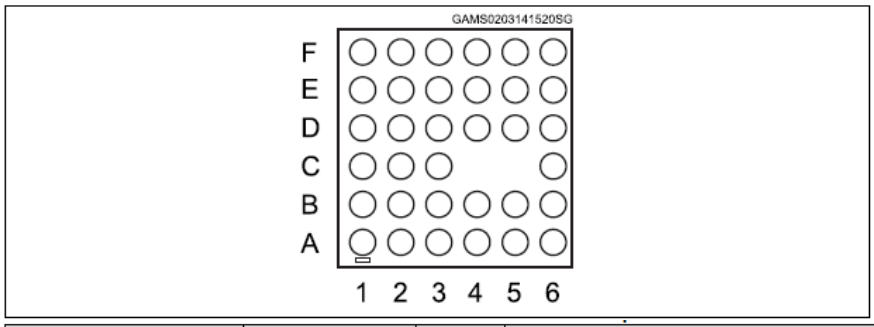
6.1 Device details

6.1.1 Pin connection

BLUENRGMSQTR

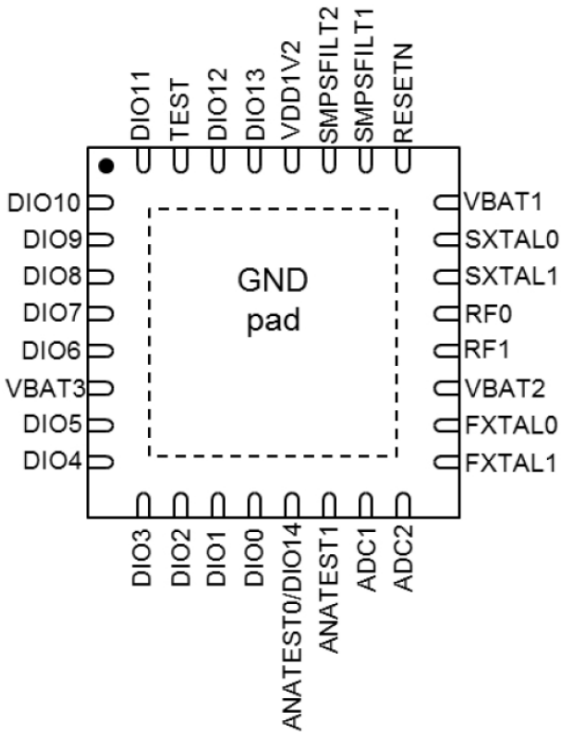


BLUENRGMSQTR

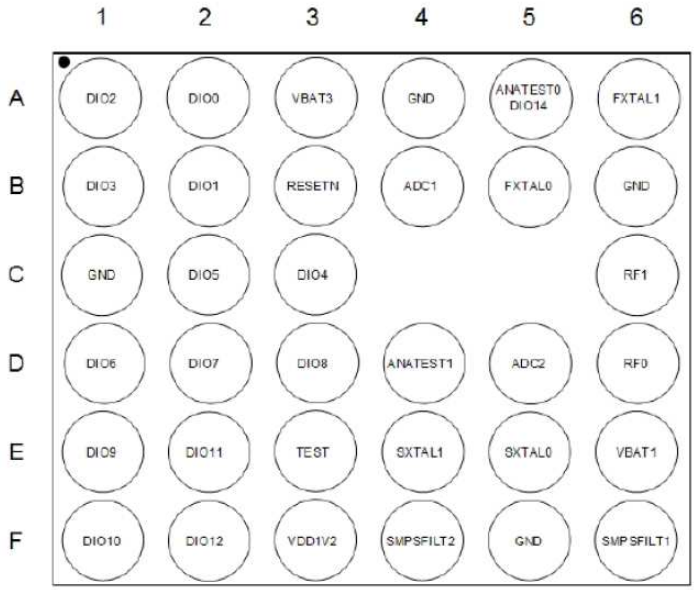


Pins		Name	I/O	Description
QFN32	WLCSP			
1	E2	SPI_MOSI	I	SPI_MOSI
2	E1	SPI_CLK	I	SPI_CLK
3	D2	SPI_IRQ	O	SPI_IRQ
4	D1	TEST1	I/O	Test pin
5	C1	VBAT3	VDD	1.7-3.6 battery voltage input
6	C2	TEST2	I/O	Test pin connected to GND
7	B1	TEST3	I/O	Test pin connected to GND
8	B2	TEST4	I/O	Test pin connected to GND
9	A1	TEST5	I/O	Test pin connected to GND
10	B3	TEST6	I/O	Test pin connected to GND
11	A2	TEST7	I/O	Test pin connected to GND
12	A3	VDD1V8	O	1.8 V digital core
13	A4	TEST8	I/O	Test pin not connected
14	A5	TEST9	I/O	Test pin not connected
15	B4	TEST11	I/O	Test pin not connected (QFN32) Test pin connected to GND (WLCSP)
16	B5	TEST12	I/O	Test pin not connected (QFN32) Test pin connected to GND (WLCSP)
17	A6	FXTAL1	I	16/32 MHz crystal
18	B6	FXTAL0	I	16/32 MHz crystal
19	-	VBAT2	VDD	1.8-3.6 battery voltage input
20	C6	RF1	I/O	Antenna + matching circuit
21	D6	RF0	I/O	Antenna + matching circuit
22	E6	SXTAL1	I	32 kHz crystal
23	E5	SXTAL0	I	32 kHz crystal
24	D5	VBAT1	VDD	1.7-3.6 battery voltage input
25	E4	RESETN	I	Reset
26	F6	SMPSFILT1	O	SMPS output
27	-	NO_SMPS	I	Power management strategy selection
28	F5	SMPSFILT2	I/O	SMPS input/output
29	F3	VDD1V2	O	1.2 V digital core
30	E3	TEST10	I/O	TEST pin connected to GND
31	F2	SPI_CS	I	SPI_CS
32	F1	SPI_MISO	O	SPI_MISO
-	C3	GND	GND	Ground
-	D3	GND	GND	Ground
-	D4	GND	GND	Ground
-	F4	SMPS-GND	GND	SMPS ground

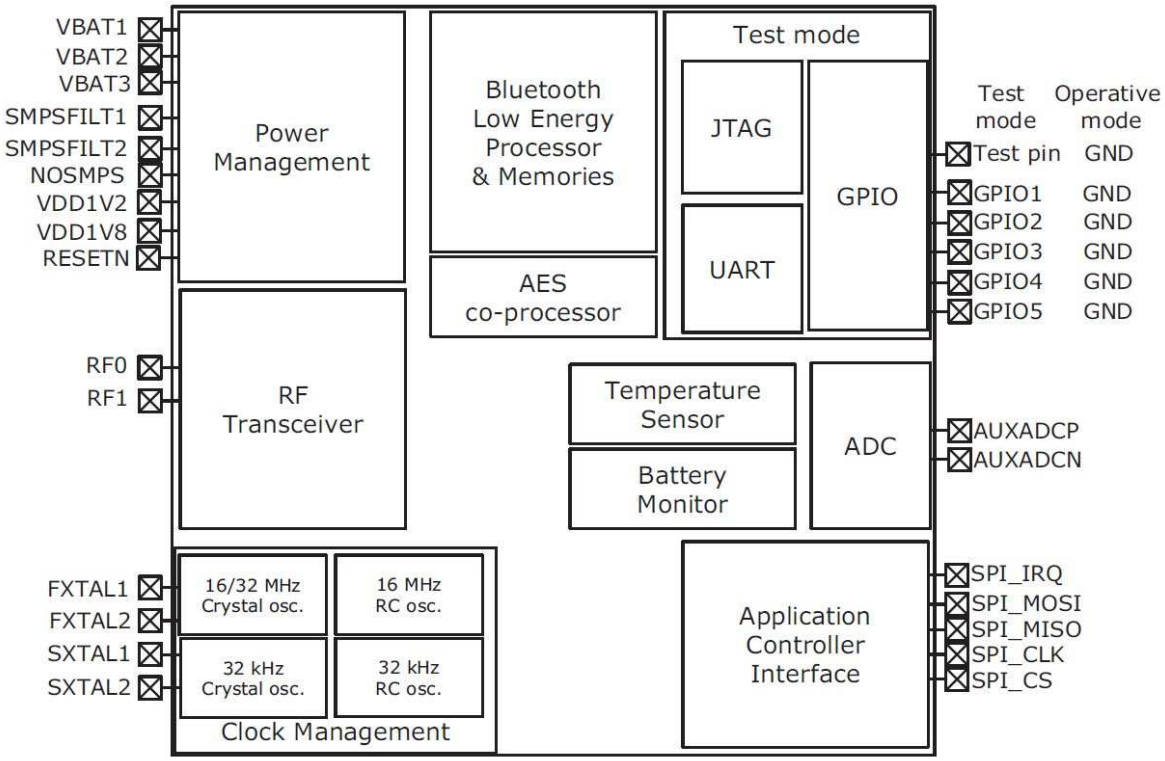
BUENRG-132



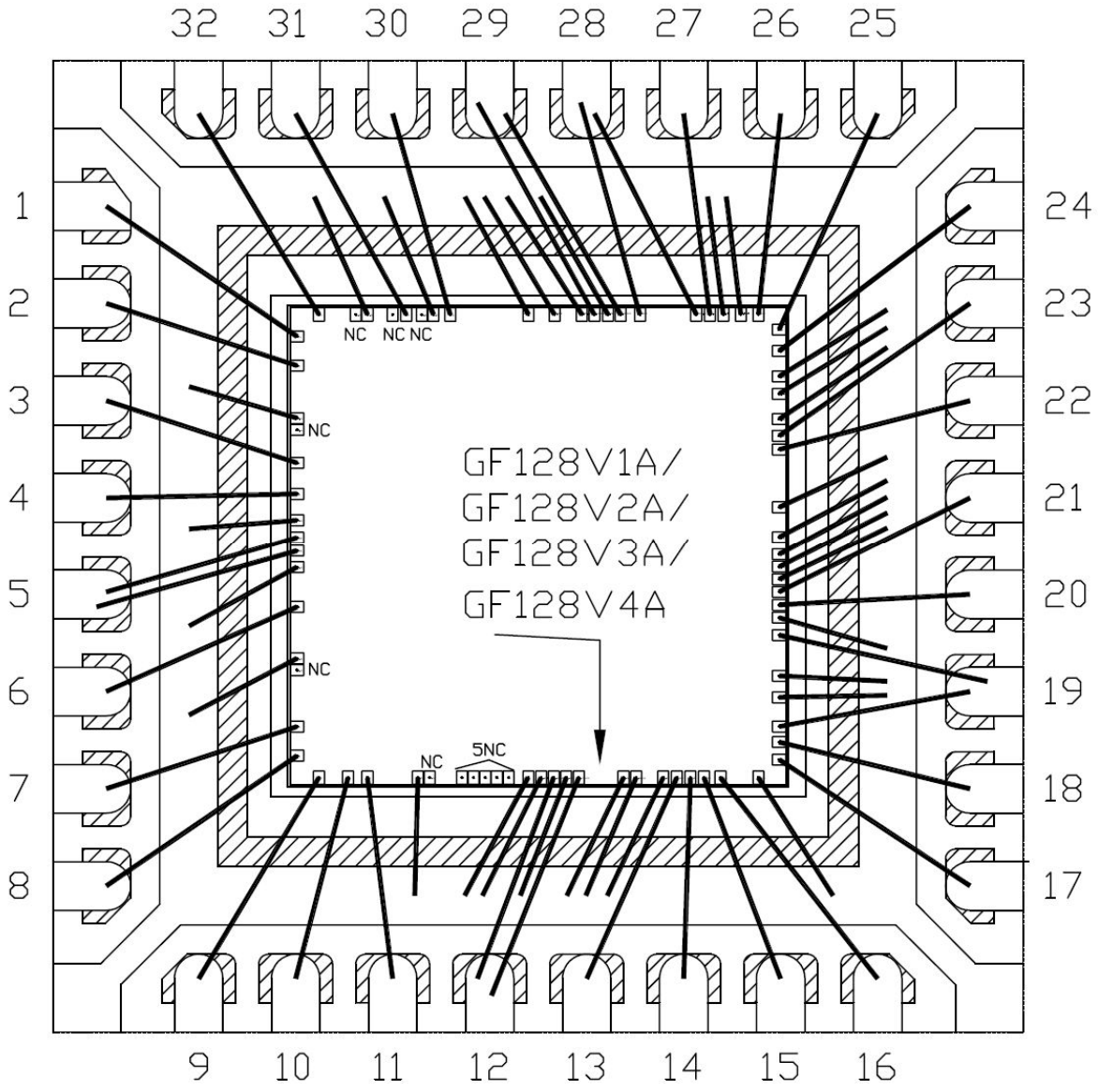
BLUENRG-134



Block diagram



6.1.2 Bonding diagram



6.1.4 Package outline/Mechanical data

DOCUMENT 8362854 REVISION A CONTROLLED DOCUMENT (Check latest revision) DATE 18-NOV-2011 page: 1/2

Check latest version

PACKAGE OUTLINE ASSEMBLY

TITLE: VFQFPN 5X5X0.9 3.6X3.6 EP 32L 0.5P

PACKAGE CODE: A0K1

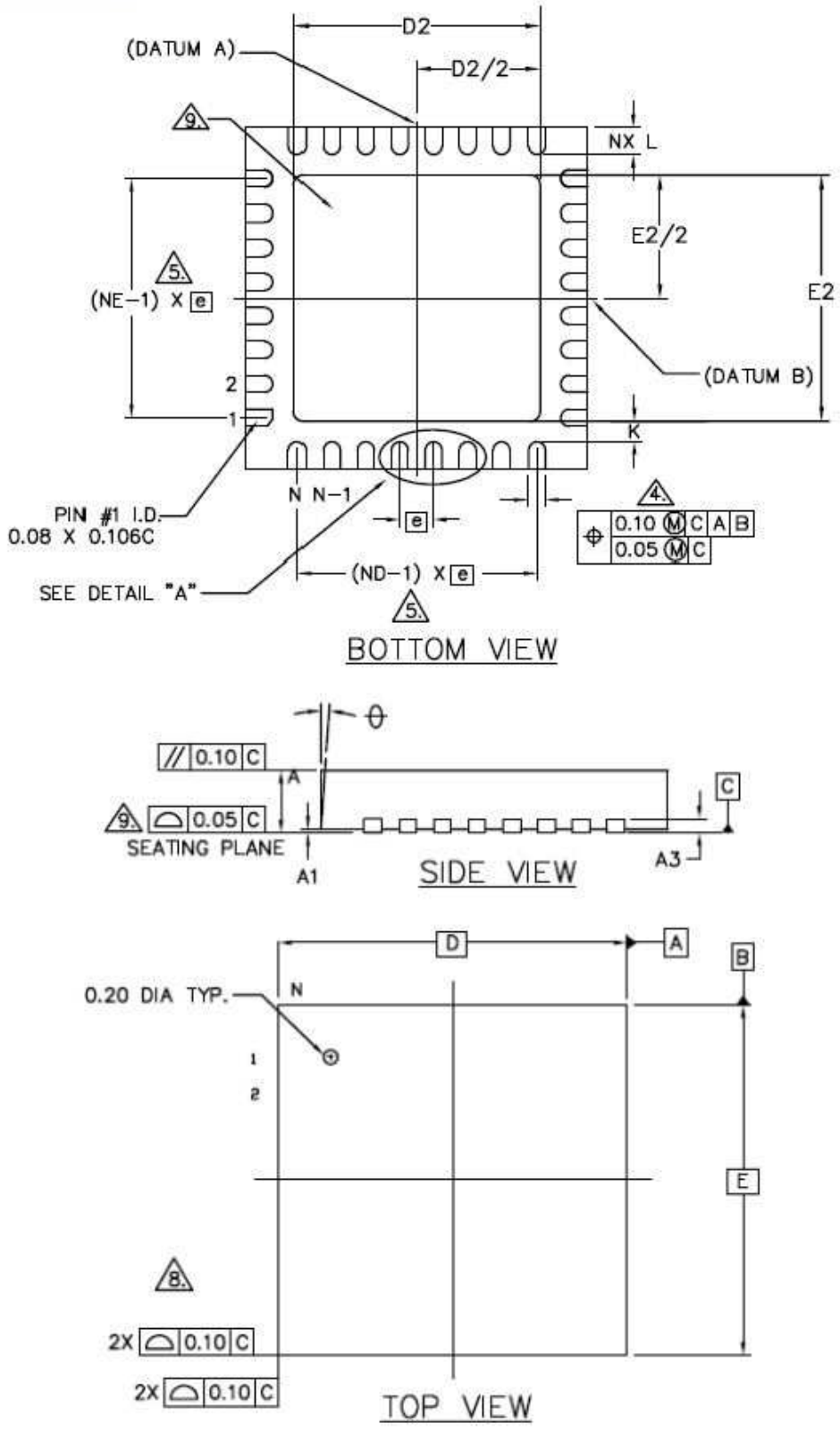
JEDEC/EIAJ REFERENCE NUMBER: MO-220K / VARIATION VHHD-5 (THERMALLY ENHANCED PLASTIC ULTRA THIN AND EXTRA THIN FINE PITCH QUAD FLAT NO- LEAD PACKAGE)

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A	0.80	0.85	1.0	0.80	0.85	0.90	
A1	0.0	0.02	0.05	0.0	0.02	0.05	
A3		0.20 REF			0.203 REF		
b	0.25	0.25	0.30	0.18	0.25	0.30	(4)
D		5.00 BSC			5.00 BSC		
E		5.00 BSC			5.00 BSC		
D2	3.2	--	3.70	3.50	3.60	3.70	
E2	3.2	--	3.70	3.50	3.60	3.70	
e		0.50 BSC			0.50 BSC		
L	0.30	0.40	0.50	0.35	0.40	0.45	
Φ	0°		14°	0°	--	12°	2
K	0.20	--	--	0.20	--	-	

NOTES:

(1) Dimensioning and tolerancing conforme to ASME Y14.5M – 1994
(2) All dimensions are in millimeters, Φ is in degrees.
(3) Max. package warpage is 0.05mm.
(4) Dimension b applies to metalized terminal and is measured between radius on the other end of the terminal, the dimension b should not be measured in that radius area.
(5) Maximum allowable burrs is 0.076mm in all directions.
(6) Pin #1 on top will be laser marked.

Check latest version



TITLE: WLCSP 2.69x2.56x0.5 34 PITCH 0.4 BALL 0.25

PACKAGE CODE: 01C1 (F157)

JEDEC/EIAJ REFERENCE NUMBER: N/A

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A		0.50	0.52		0.50	0.52	
A1	0.16	0.175	0.19	0.16	0.175	0.19	
A2		0.022	0.025		0.022	0.025	
A3	0.285	0.30	0.315	0.285	0.30	0.315	
b		0.27			0.27		(2)
D	2.50	2.56	2.58	2.50	2.56	2.58	(3)
D1		2.00			2.00		
E	2.63	2.69	2.71	2.63	2.69	2.71	(4)
E1		2.00			2.00		
e		0.40			0.40		
f		0.28			0.28		
g		0.35			0.35		
ccc			0.05			0.05	

NOTES:

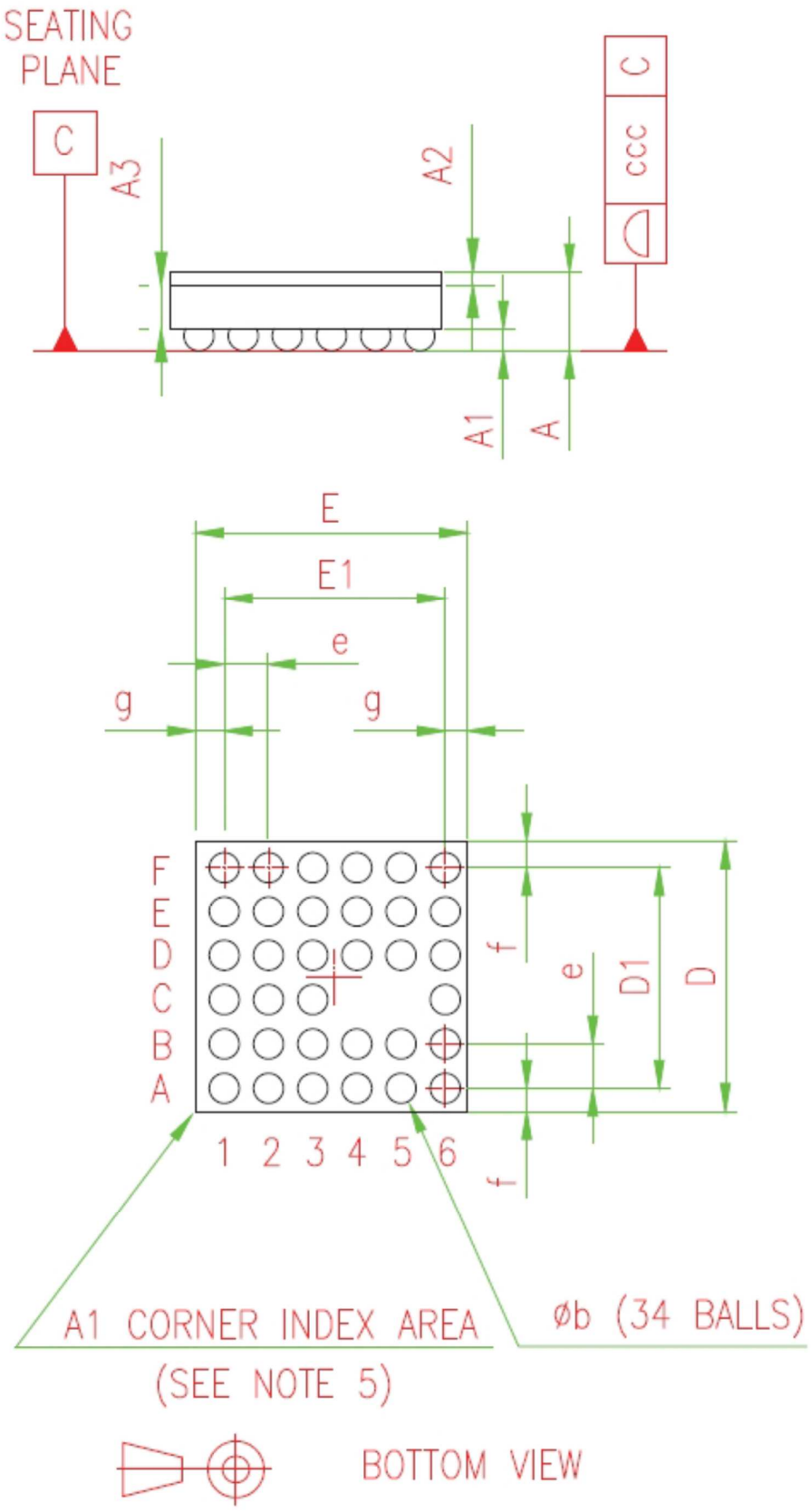
(1) – WLCSP stands for **W**afer **L**evel **C**hip **S**cale **P**ackage.

(2) – The typical ball diameter before mounting is 0.25mm.

(3) – D=f+D1+f.

(4) – E=g+E1+g.

(5) – The terminal A1 corner must be identified on the top surface by using a laser marking dot.


SEATING
PLANE
C
A3
A2
ccc
C
A1
A
E
E1
e
g
g
F
E
D
C
B
A
1 2 3 4 5 6
f
e
D1
D
f
A1 CORNER INDEX AREA
(SEE NOTE 5)
øb (34 BALLS)
BOTTOM VIEW

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.