

PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.		MDG/17/10270
1.3 Title of PCN		Additional Amkor ATT (Taiwan) back-end site - STM32L073x 192K products in WLCSP package
1.4 Product Category		STM32L073x 192K products in WLCSP
1.5 Issue date		2017-12-04

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Michel BUFFA
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	Amkor ATT (Taiwan)

4. Description of change

	Old	New
4.1 Description	Back-end plant : - Stats ChipPAC SCS (Singapore)	Back-end plants : - Stats ChipPAC SCS (Singapore) - existing source - Amkor ATT (Taiwan) - additional source - Same Bill of Materials (BOM) - Line already in production
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	no change	

5. Reason / motivation for change

5.1 Motivation	Those changes will improve and secure service through double-sourcing.
5.2 Customer Benefit	DOUBLE SOURCING

6. Marking of parts / traceability of change

6.1 Description	The marking composition indicated on the products is changing : - Country Of Origin changes from SGP (Singapore) to TWN (Taiwan)
-----------------	---

7. Timing / schedule

7.1 Date of qualification results	2017-11-29
7.2 Intended start of delivery	2018-03-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	10270 MDG-MCD RER1412 V1.1- PCN8460 PCN10270- Additional Amkor ATT site for WL..._.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2017-12-04

9. Attachments (additional documentations)

10270 Public product.pdf
10270 PCN10270_Additional information.pdf
10270 MDG-MCD RER1412 V1.1- PCN8460 PCN10270- Additional Amkor ATT site for WL....pdf

10. Affected parts

10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STM32L082CZY6TR	

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

MMS Reliability Evaluation Report

RERMCD1412

*Qualification of AMKOR second source
back-end sites
STM32 in WLCSP- 8" wafers
(PCN 8460- PCN10270)*

General Information		Locations	
Product division	MMS MCD	Assembly plant location	AMKOR Taiwan - ATT5 (Bumping) - ATT3 (DPS)
Package Description	8" WLCSP	Reliability Evaluation assessment	PASS

Reliability tests are performed to assess package integrity under extreme physical and electrical conditions.

They guarantee product/package reliability during end-application manufacturing and operation.

Methodology for product maturity approval has been performed in accordance to STMicroelectronics standard operating procedures (SOP).

Date	Revision	Changes
August 12 th , 2014	1.0	Initial release
November 02 nd , 2017	1.1	Data for STM32L073xx added for PCN 10270

Approval List			
Function	Site	Name	Date
MMS BE Q&R Responsible	ST Rousset	Antoine GARCIA	Aug 12, 2014
MCD Quality Manager	ST Rousset	Pascal NARCHE	Aug 12, 2014
MCD Quality Manager	ST Rousset	Pascal NARCHE	Nov 02, 2017

TABLE OF CONTENTS

MMS RELIABILITY EVALUATION REPORT	1
RERMCD1412	1
1 RELIABILITY EVALUATION OVERVIEW	3
1.1 OBJECTIVES	3
1.2 CONCLUSION	3
2 PACKAGE CHARACTERISTICS	4
2.1 TEST VEHICLE PACKAGE DESCRIPTION (ABSTRACT FROM DEVICE DATASHEET):	4
2.2 TRACEABILITY	6
2.2.1 <i>Wafer fab information</i>	6
2.2.2 <i>Assembly information</i>	6
3 RELIABILITY EVALUATION PLAN/ RESULTS	8
3.1 RELIABILITY EVALUATION RESULTS SUMMARY	8
3.2 PACKAGE ORIENTED TESTS	9
3.2.1 <i>Trials description</i>	9
4 APPLICABLE AND REFERENCE DOCUMENTS	11
5 GLOSSARY	11

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

In order to sustain strong demand and in order to provide best-in-class service to his customers, ST MCD Division has decided to increase capacity through double-sourcing for 8" wafers WLCSP assembly.

Target of this reliability evaluation is to qualify AMKOR Taiwan as 2nd 8" wafers WLCSP assembly source:

- Assembly site: AMKOR ATT5
- Test & Finishing site: AMKOR ATT3

3 test vehicles have been identified to cover this reliability evaluation:

- STM32F072xx (TSMC 0.18µm Front-End technology): WLCSP 49 balls
- STM32L151xx (ST F9GO2S Front-End technology): WLCSP 63 balls
- STM32L073xx (ST F9GO2S Front-End technology): WLCSP 49 balls

1.2 Conclusion

All package oriented reliability trials conducted on the 3 test vehicles have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

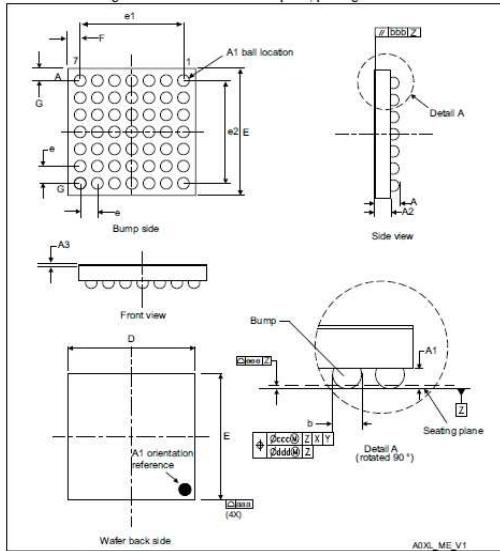
AMKOR Taiwan is qualified as 2nd 8" wafers WLCSP assembly source.

Refer to section [3.1 Reliability Evaluation results summary](#) for reliability evaluation detailed results.

2 PACKAGE CHARACTERISTICS

2.1 Test Vehicle Package description (Abstract from device datasheet):

STM32F072xx (TSMC 0.18µm Front-End technology): WLCSP 49 balls 0.4mm pitch



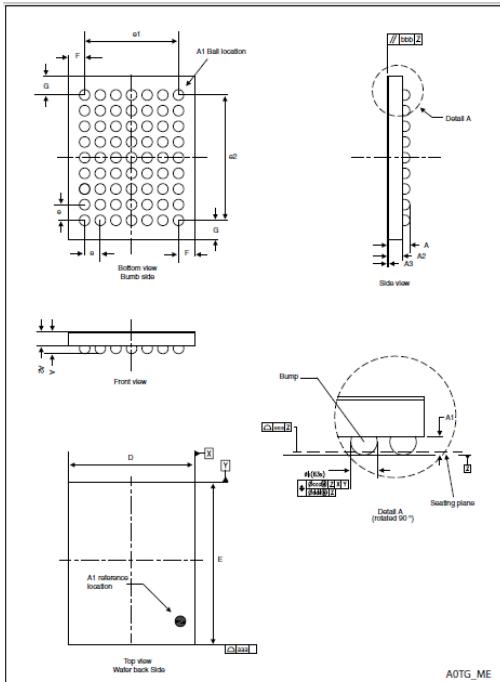
1. Drawing is not to scale.

2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.242	3.277	3.312	0.1276	0.1290	0.1304
E	3.074	3.109	3.144	0.1210	0.1224	0.1238
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.438	-	-	0.0173	-
G	-	0.354	-	-	0.0140	-
N	49					
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

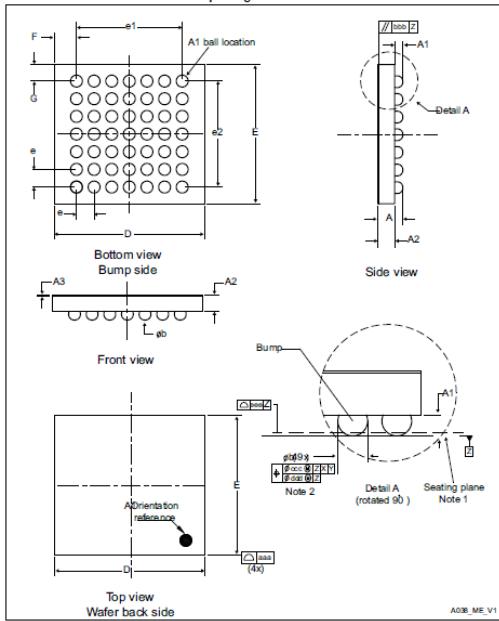
STM32L151xx (ST F9GO2S Front-End technology): WLCSP 63 balls 0.4mm pitch



1 Drawing is not to scale.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0213	0.0224	0.0236
A1		0.190			0.0075	
A2		0.380			0.0150	
A3		0.025			0.0010	
Øb	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	3.193	3.228	3.263	0.1257	0.1271	0.1285
E	4.129	4.164	4.199	0.1626	0.1639	0.1653
e		0.400			0.0157	
e1		2.400			0.0945	
e2		3.200			0.1200	
F		0.414			0.0163	
G		0.482			0.0190	
aaa			0.100			0.0039
bbb			0.100			0.0039
ccc			0.100			0.0039
ddd			0.050			0.0020
eee			0.050			0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

STM32L073xx (ST F9GO2S Front-End technology): WLCSP 49 balls 0.4mm pitch


1. Drawing is not to scale.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.259	3.294	3.329	0.1283	0.1297	0.1311
E	3.223	3.258	3.293	0.1269	0.1283	0.1296
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.447	-	-	0.0176	-
G	-	0.429	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

2.2 Traceability

2.2.1 Wafer fab information

- **STM32F072xx: WLCSP 49 balls 0.4mm pitch**
 - o Wafer fab manufacturing location : TSMC Fab11
 - o Silicon process technology: 0.18µm Gen.Emb.Flash logic
- **STM32L151xx: WLCSP 63 balls 0.4mm pitch**
 - o Wafer fab manufacturing location : ST Rousset
 - o Silicon process technology : F9GO2S (CMOSF9S)
- **STM32L073xx: WLCSP 49 balls 0.4mm pitch**
 - o Wafer fab manufacturing location : ST Rousset
 - o Silicon process technology : F9GO2S (CMOSF9S)

2.2.2 Assembly information

- **STM32F072xx:**
 - o Assembly site : AMKOR Taiwan
 - Bumping : ATT5
 - Test & finishing : ATT3
 - o Package description : WLCSP49 0.4mm pitch
 - o Die thickness after back-grinding : 355+/-12.5 µm
 - o Balls material & diameter : SACN125 (balls raw diameter 230µm)
 - o Passivation material : Polyimide
 - o Redistribution material : Copper RDL + TiW/Cu/Cu UBM
 - o Back side coating material : PET film
 - o Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1
- **STM32L151xx:**
 - o Assembly site : AMKOR Taiwan
 - Bumping : ATT5
 - Test & finishing : ATT3
 - o Package description : WLCSP63 0.4mm pitch
 - o Die thickness after back-grinding : 355+/-12.5 µm
 - o Balls material & diameter : SACN125 (balls raw diameter 250µm)
 - o Passivation material : Polyimide
 - o Redistribution material : Copper RDL + TiW/Cu/Cu UBM
 - o Back side coating material : PET film
 - o Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1

- **STM32L073xx:**

- o Assembly site : AMKOR Taiwan
 - Bumping : ATT5
 - Test & finishing : ATT3
- o Package description : WLCSP49 0.4mm pitch
- o Die thickness after back-grinding : 355+/-12.5 μ m
- o Balls material & diameter : SACN125 (balls raw diameter 230 μ m)
- o Passivation material : Polyimide
- o Redistribution material : Copper RDL + TiW/Cu/Cu UBM
- o Back side coating material : PET film
- o Package Moisture Sensitivity Level (JEDEC J-STD020D): MSL1

3 RELIABILITY EVALUATION PLAN/ RESULTS

Package integrity of test vehicles described in above section has been evaluated through below reliability trials.

3.1 Reliability Evaluation results summary

Reliability trials have been performed on 4 assembly lots:

Die	Device	Package	Reduced Rawline	Number of lots	RELIS ref
448	STM32F072x	WLCSP49	3D*448	2	GRAL1414001/1414002
427	STM32L151xx	WLCSP63	TB*427	2	GRAL1414003/1414004
447	STM32L073xx	WLCSP49	51*447	1	GRAL1737003

Package oriented trials - Short description						Results				
Descript.	Test/Method	Conditions	Sample Size	Criteria	Read out /Duration	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5
<i>ESD Charge Device Model</i>										
ESD CDM	ANSI/ESD STM5.3.1	N.A	3 X 2	Class 3	250V	0/3	-	-	-	
				Class 4	500V	-	-	0/3	-	0/3
<i>Preconditioning: moisture sensitivity level 1</i>										
PC	J-STD-020D JESD22-A113	24h bake @ 125°C 168h @ 85°C / 85% RH Reflow simulation (3 times) @ 260°C peak temperature	308 X 4	A0/R1 (*)		0/308	0/308	0/308	0/308	NA
<i>Temperature Humidity Bias after Preconditioning</i>										
THB	JESD 22-A101	85°C, 85% RH	77 X 4	A0/R1 1000h	1000h	0/77	0/77	0/77	0/77	NA
<i>Unbiased HAST after Preconditioning</i>										
UHAST	JESD 22-A118	Ta=130°C 85%RH	77 X 4	A0/R1 96h	96h	0/77	0/77	0/77	0/77	NA
<i>Thermal Cycling after Preconditioning</i>										
TC	JESD 22-A104	-65°C/+150°C	77 X 4	A0/R1 1000cy	500cy	0/77	0/77	0/77	0/77	NA
<i>High Temperature Storage Life after Preconditioning</i>										
HTSL	JESD 22-A103	150°C	77 X 4	A0/R1 1000h	1000h	0/77	0/77	0/77	0/77	NA

(*) A0/R1: Accepted if 0 reject/ Rejected if 1 reject.

3.2 Package oriented tests

3.2.1 Trials description

3.2.1.1 Preconditioning (PC)

According to ST spec 0098044.

Preconditioning test sequence simulates storage and soldering of SMD (surface mount devices) before submitting them to the reliability tests. It aims to validate the moisture sensitivity level of the package, and prepare it to the stress of additional reliability tests, thus enabling a good modelization of the life of the packaged product.

Out-of-bag floor life storage and soldering are modeled by the following test sequence:

- Bake to completely remove moisture from the package;
- Moisture soak according to the package moisture level;
- IR reflow.

The aim is to check that the chip and plastic package withstand the stress due to report on card. Depending on their technology, packages may absorb moisture during their transportation and/or storage, moisture that is released during the soldering operation. At this step, the moisture absorbed is vaporized due to high temperature of solder report process. This phenomenon can create plastic swelling, "pop corn" effect, and cracks which eventually results in wire breakage, passivation cracks, and delamination.

3.2.1.2 Unbiased Highly Accelerated Stress Test (uHAST)

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solidstate devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

3.2.1.3 High Temperature Storage Life (HTSL)

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

Purpose: to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.

3.2.1.4 Temperature Cycling (TC)

The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere (thermal gradient typical 10 C/min).

Purpose: to investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system.

Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation.

3.2.1.5 Temperature Humidity Bias (THB)

The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.

The Temperature Humidity Bias follows the same method than HAST at lower temperature.

Purpose: to investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions.

Typical failure mechanisms are electro-chemical corrosion and surface effects related to the molding compound.

The package moisture resistance with electrical field applied is verified, both electrolytic and galvanic corrosion are put in evidence.

Conditions:

- $T_a = 85^\circ\text{C}$; R.H.=85%;
- Power supply voltage less or equal to max operative voltage to not exceed $T_j = 95^\circ\text{C}$.

3.2.1.6 ESD Charge Device Model (CDM)

This ESD failure model is associated with the device and package itself. The CDM is intended to simulate charging/discharging events that occur in production equipment and processes. The Field induced CDM equivalent circuit used to describe this phenomenon is illustrated in Figure 1.

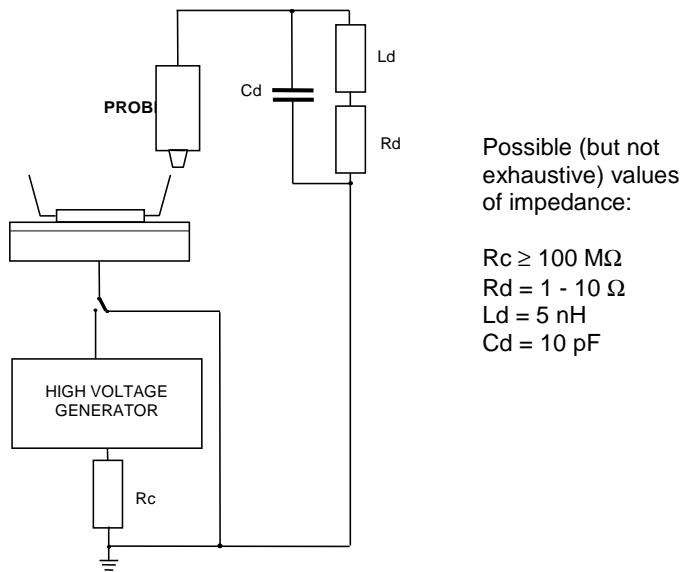


Fig.1 : Field induced CDM equivalent circuit

4 APPLICABLE AND REFERENCE DOCUMENTS

- ADCS 0061692: RELIABILITY TESTS AND CRITERIA FOR QUALIFICATIONS
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.7: Product Maturity Level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.19: Process maturity level
- ANSI-ESD STM5.3.1: Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
- JESD22-A103: High temperature storage life
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A118: Accelerated moisture resistance - unbiased hast
- JESD22-A104: Temperature cycling

5 GLOSSARY

ESD CDM	Electrostatic discharge (charge device model)
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
UHAST	Unbiased HAST
HTSL	High temperature storage life

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com