PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APM-PWR/10/5595
Notification Date 05/17/2010

MDmesh IITM Technology, Power MOSFET Transistors,

Front-end Capacity Extension - M5 Wafer FAB, Catania (Italy)

Table 1. Change Implementation Schedule

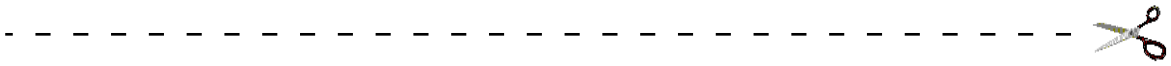
Forecasted implementation date for change	10-May-2010
Forecasted availabillity date of samples for customer	10-May-2010
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-May-2010
Estimated date of changed product first shipment	16-Aug-2010

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Waferfab process change
Reason for change	Capacity Extension
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power MOSFET productivity, this document is announcing that MDmesh IITM Technology of Power MOSFET Transistors will be manufactured also in the M5 Wafer FAB Catania (Italy). MDmesh IITM Technology production, guarantees the same quality and electrical characteristics as the current ST's Ang Mo Kio (Singapore) wafer FAB. Devices used for qualification are available as Samples.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	See "V5" as Wafer FAB production area code printed on the box label.
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APM-PWR/10/5595**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 05/17/2010**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Division Marketing Manager
Wilson, Ian	Division Product Manager
Falcone, Giuseppe	Division Q.A. Manager

Dear Customer,

Please be informed that MDmesh II™ Technology of Power MOSFET Transistors, manufactured in the ST's Ang Mo Kio (Singapore) FAB, will be manufactured also in the M5 Wafer FAB Catania (Italy).

The involved product series and affected packages are listed in the table below:

Product Family Code	Product Family Description	Package	Commercial Product / Series
29	Power MOSFET Transistors	All	See attached list

Any other Product related to the above series, manufactured in the M5 Wafer FAB Catania (Italy), even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 18-2010.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Code	Product Family Description	Package	Part Number - Test Vehicle
29	Power MOSFET Transistors	All	STP13NM60N

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	Production Start	1st Shipments
Power MOSFET Transistors	From Week 18-2010	From Week 31-2010

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipments may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of MDmesh II™ Technology of Power MOSFET Transistors, manufactured in the M5 Wafer FAB Catania (Italy), will be ensured by “V5" as Wafer FAB production area code printed on the box label.

Sincerely Yours.

Reliability Report

On

MDmesh II™ Technology Power MOSFET Transistors made in M5 Wafer FAB, Catania (Italy), for Front-end Capacity Extension

General Information	
Product Lines	M263
Product Description	Power MOSFET
Commercial Products	STP13NM60N
Product Group	IMS - APM
Product division	Power MOSFET
Package	TO-220
Silicon Process technology	Power MOSFET MDmesh II™

Locations	
Wafer fab	*M5 Wafer FAB - Catania (Italy)*
Assembly plant	*BOUSKOURA (MOROCCO)*
Reliability Lab	*IMS-APM Catania Reliability Lab*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	April-2010	6	G.Montalto	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualifications of the MDmesh II™ Technology Power MOSFET Transistors made in M5 Wafer FAB, Catania (Italy), for Front-end Capacity Extension.

3.2 Conclusion

The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Power MOSFET MDmesh II™

4.2 Construction note

D.U.T.: STP13NM60N LINE: M263 PACKAGE: TO-220

Wafer/Die fab. information	
Wafer fab manufacturing location	*M5 Catania (ITALY)*
Technology	MDmesh II™
Die finishing back side	Ti/Ni/Au
Die size	3950 x 2930 µm^2
Metal	Al/Si
Passivation type	NITRIDE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*M5 Catania (ITALY)*
Test program	According to specification

Assembly information	
Assembly site	*BOUSKOURA (MOROCCO)*
Package description	TO-220
Molding compound	Epoxy Resin
Frame material	Copper (Ni/Ni-P plated)
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Gate Al 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	*BOUSKOURA (MOROCCO)*
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STP13NM60N	M263	Power MOSFET

5.2 Reliability test plan and results summary

D.U.T.: STP13NM60N LINE: M263 PACKAGE: TO-220

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
HTSL	N	JESD22 A-103	TA=150℃	77	1000H	0/77
HTRB	N	JESD22 A-108	TA = 125℃, Vbias=480V	77	1000H	0/77
HTGB	N	JESD22 A-108	Tj=150℃, Vbias=20V	77	1000H	0/77
THB	N	JESD22 A-101	TA = 85℃, RH = 85%, Vbias=100V	77	1000H	0/77
TC	N	JESD22 A-104	TA=-65℃ TO +150℃	77	500 cy	0/77
TF	N	Mil-Std 750D Method 1037	ΔTC=105℃ - Pd=4.75W	50	10 kcy	0/50
AC	N	JESD22 A-102	Pa=2Atm / Ta=121℃	77	96 H	0/77

ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF	This test is performed to demonstrate the quality and reliability of devices exposed to cyclic variation in electrical stress between "on" and "off" conditions and resultant cyclic variation in device and case temperatures (thermo-mechanical stress).	The purpose of this test is to detect assembly defects: improper die-attach, bonding weakness and thermal mismatch among various components of the package.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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