



Product Change Notification - SYST-31QEFB481

Date:

04 Feb 2020

Product Category:

32-bit Microcontrollers

Affected CPNs:**Notification subject:**

Data Sheet - SAM C20/C21 Family Data Sheet

Notification text:

SYST-31QEFB481

Microchip has released a new Product Documents for the SAM C20/C21 Family Data Sheet of devices. If you are using one of these devices please read the document located at [SAM C20/C21 Family Data Sheet](#).

Notification Status: Final

Description of Change: This revision includes the following changes

Section Name	Update Description
Configuration Summary	<ul style="list-style-type: none">Updated Table 1-3 SAM C21 Family Features with new values for the PTC
Block Diagram	<ul style="list-style-type: none">Updated Table 1-4 SAM C20 Family Features with new values for the AC <p>Updated the arrow to bridge between PORT and AHB- APB Bridge B.</p>
Signal Descriptions	Updated Table 5-1 Signal Descriptions List - SAM C20/C21 with small typographical edits for VOUT and VREFA.
Multiplexed Signals	Updated Table 6-1, Table 6-2, Table 6-3, and Table 6-4 with new ADC-DAC/VREFA values in the REF column.
Processor and Architecture	Updated Table 10-3 and 10-4 in Interrupt Line Mapping with notations designating which chip the Peripheral Source applies to.
GCLK	<ul style="list-style-type: none">Updated Figure 16-1 Block Diagram to correct missing information <ul style="list-style-type: none">Updated the GENCTRL bit for the SYNCBUSY register
MCLK	<ul style="list-style-type: none">Updated the AHBMASK Register to display the DIVAS and APBD bits <ul style="list-style-type: none">Updated the TC4 bit of the APBCMASK Register to display the Description table <ul style="list-style-type: none">Updated the APBDMASK Register with a new note on availability of features for SAMC2x "N" Series devices
PM	Updated the SLEEPMODE bit of the SLEEPCFG Register with new data in the table.

OSCCTRL	Updated the AMPGC bit of the XOSCCTRL Register with a new note.
SUPC	<ul style="list-style-type: none"> • Updated Voltage Reference System Operation with new text referencing the INTREF • Updated Selecting a Voltage Reference with new text for the INTREF • Updated the ACTCFG bit of the BODVDD Register to remove an erroneous reference to Sleep Mode • Updated the STDBYCFG bit of the BODVDD Register with new table values
EIC	Updated the LOCK Register with new reset values.
NVMCTRL	
PORT I/O Pin Controller	Corrected typographical error in OUTTGL reference in Features.
CAN	<ul style="list-style-type: none"> • Updated Power Management with new interrupt text • Updated Sleep Mode Operation with new introductory sentence
CCL	<ul style="list-style-type: none"> • Updated Truth Table Inputs Selection for Internal Events Inputs Selection (EVENT) with C20/C21 availability text • Updated the table for the INSELx bit in the LUTCTRLn Register
ADC	<ul style="list-style-type: none"> • Updated Overview with supporting text for the INTREF voltage reference • Updated Features with new supporting text for INTREF • Updated Analog Connections with new supporting text for INTREF • Updated Reference Configuration with new supporting text for INTREF • Updated the REFSEL bit for the REFCTRL

	<p>Register</p> <ul style="list-style-type: none"> Updated the MUXPOS bit for the INPUTCTRL Register
<p>SDADC</p> <p>AC</p>	<ul style="list-style-type: none"> Removed erroneous information from Features for Conversion Range Updated the REFSEL bit for the REFCTRL Register Updated the Overview with information for CMP2 and CMP3 on E and G variants Updated Features with information on the INTREF Updated the Block Diagrams to replace Bandgap with INTREF Updated Analog Connections to replace Bandgap text with INTREF Updated Principle of Operation to replace Bandgap text with INTREF Updated the table for the MUXNEG bit of the COMPCTRL Register
<p>DAC</p> <p>FREQM</p>	<ul style="list-style-type: none"> Updated Analog Connections to replace Bandgap text with INTREF Updated the table for the REFSEL bit for the CTRLB Register Added a new note to the Block Diagram Updated the DIVREF bit description for the CFGA Register
<p>Electrical Characteristics at 85°C</p>	<ul style="list-style-type: none"> Updated Table 45-18 Decoupling Requirements in Voltage Regulator Characteristics with new values and a new note Updated Table 45-19 Operating Conditions in Analog-to-Digital Converter (ADC) Characteristics with INTREF replacing Bandgap

	<ul style="list-style-type: none"> Updated Table 45-23 Operating Conditions in Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics with the addition of a note and the removal of single-ended mode references Updated Crystal Oscillator Characteristics with a new equation and removed CSHUNT from the diagram
Electrical Characteristics at 105°C	Updated Table 47-8 Operating Conditions in Sigma-Delta Analog-to-Digital Converter (SDADC) Characteristics to remove the Single-ended mode reference and added new note.
AEC Q100 Grade 1, Electrical Characteristics at 125°C	Updated Table 48-3 Current Consumption with new values for the Maximum under Standby.
Schematic Checklist	Removed pF references from Figure 50-7 Crystal Oscillator Schematic and removed pF references from Table 50-5 in Crystal Oscillator

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 04 Feb 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[SAM C20/C21 Family Data Sheet](#)

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