MICROCHIP

Product Change Notification - SYST-17YMPV099

Date:

18 Feb 2020

Product Category:

Microprocessors

Affected CPNs:

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Notification subject:

Data Sheet - SAM9X60 Datasheet

Notification text:

SYST-17YMPV099

Microchip has released a new Product Documents for the SAM9X60 Datasheet of devices. If you are using one of these devices please read the document located at **SAM9X60 Datasheet**.

Notification Status: Final

Description of Change:
1. All section: Changes: Changed order of bits (now from MSB to LSB) in Register Summary tables
2. Safety and Security Features Removed section: "Classical Advanced Software Crypto Library (CASCL)" from Security Features table
3. Peripherals section: Updated FLEXCOM Features table
4. Boot Strategies section: Updated NAND Flash Boot: NAND Flash Detection introduction OTP Memory Controller (OTPC) OTPC_CR: updated READ bit description
5. Clock Generator section: Updated Main Clock (MAINCK) Block Diagram
6. Power Management Controller (PMC) section: Updated General Clock Distribution Block Diagram and List of write-protected registers in Register Write Protection. PMC_CPU_CKR: corrected MDIV field width
7. External Bus Interface (EBI) section: Updated Multi-Port DDR and SDRAM Controllers
8. AHB Multiport DDR-SDRAM Controller (MPDDRC) section: DDR2-SDRAM Initialization: added TRFC constraint content. Monitor: added monitor use example. Updated: Quality Of Service Arbitration, Description, Change Frequency During Self-Refresh Mode with Low-power DDR-SDRAM Devices.
9. Flexible Serial Communication Controller (FLEXCOM) section: Added introduction in USART FIFO Mode Register. USART FIFO Level Register, USART FIFO Interrupt Mask Register. SPI Status Register, SPI FIFO Mode Register, SPI FIFO Level Register, TWI FIFO Mode Register, TWI FIFO Level Register, TWI FIFO Status Register and TWI FIFO Interrupt Mask Register. Updated: Figure TWI Read Operation with Multiple Data Bytes + Write Operation with Multiple Data Bytes (Sr), TWI Clock Waveform Generator Register (CLDIV and CHDIV bit descriptions), Modes of Operation, TWI Compatibility with I2C Standard and TWI/SMBus Characteristics (Fast Mode Plus and High Speed Modes)
10. Image Sensor Interface (ISI) Power Management section: added note
11. Timer Counter (TC)section: Embedded Characteristics: corrected number of channels, Block Diagram: added Note 2, TC_SRx: corrected SECE bit position
12. Advanced Encryption Standard (AES) section: Updated Operating Modes, AES_MR (OPMOD field description) and AES_IVRx (IV field description)
13. Secure Hash Algorithm (SHA)section: SHA_MR: updated ALGO bit field description
14. True Random Number Generator (TRNG)section TRNG_PKBCR section: updated KSLAVE field description
15. Electrical Characteristics section: Updated Electrical Parameters Usage, Recommended Power Supply Sequencing introduction, ULP0 Operation and ULP1 Operation sequences of operation, Table Main RC Oscillator Characteristics and Figure Current Measurement for Applicative Use Cases
16. Mechanical Characteristics section: Updated 228-ball TFBGA Mechanical Characteristics
19. Marking section: Updated Line 4 description

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 18 February 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):
SAM9X60 Datasheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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