



Product Change Notification - SYST-09KBBY907

Date:

10 Jul 2019

Product Category:

Ethernet Switches

Affected CPNs:**Notification subject:**

Data Sheet - KSZ8567R Data Sheet Document Revision

Notification text:

SYST-09KBBY907

Microchip has released a new DeviceDoc for the KSZ8567R Data Sheet of devices. If you are using one of these devices please read the document located at [KSZ8567R Data Sheet](#).

Notification Status: Final**Description of Change:**

- 1) Table 4-15, Transmit Tail Tag Format (from Host to Switch): Bit 7 changed to 15:11 and description changed to Reserved.
- 2) Section 4.5, IEEE 1588 Precision Time Protocol: All PHY ports must be operating at 100 Mbps - or 1 Gbps removed
- 3) Section 2.1, General Description, on page 8: Updated first bullet to indicate the non-blocking wire-speed Ethernet switch fabric supports 1 Gbps on RGMII.
- 4) Section 4.3.3, Back-Off Algorithm: Updated second sentence.
- 5) Section 4.3.5, Legal Packet Size: Simplified paragraph for clarity.
- 6) Section 4.3.6, Flow Control: Simplified last sentence of third paragraph
- 7) Table 4-11: Updated Action description for the Yes entry.
- 8) Section 4.4.3.2.1, Tag Insertion and Removal: Updated last paragraph of section.
- 9) Section 4.4.8, Multiple Spanning Tree Support: Updated second sentence.
- 10) Table 4-18, ACL Matching Rule Parameters for MD = 01: Corrected ENB[1:0] 01 and 10 definitions to match those in Table 4-17, Matching Rule Options.
- 11) Section 4.5, IEEE 1588 Precision Time Protocol: Added additional paragraph to end of section.
- 12) Section 4.12, In-Band Management: a) Added to last sentence of first paragraph. b) Added additional sentence to end of second paragraph. c) Added additional sentence to end of sixth paragraph.
- 13) Section 5.1.6.17, Timestamp Control and Status Register: Updated bit 6 definition.
- 14) Section 5.2.1.7, Port Operation Control 0 Register: Updated bit 6 and 7 descriptions to include references to the MAC and additional clarification.
- 15) Section 5.2.2.12, PHY Remote Loopback Register: Simplified bit 8 description.
- 16) Section 5.2.4.1, Port MAC Control 0 Register, on page 153: Bit 0 made reserved
- 17) Section 6.4.8, Power-up and Reset Timing, on page 219: Updated Note 1.
- 18) Table 6-12: Added new trw entry to table.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 10 July 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A



Attachment(s):

[KSZ8567R Data Sheet](#)

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