Product Change Notification - SYST-06WNHS250

Date:

09 Mar 2020

Product Category:

Microprocessors

Affected CPNs:

Notification subject:

Data Sheet - SAMA5D4 Series Data Sheet

Notification text:

SYST-06WNHS250

Microchip has released a new Product Documents for the SAMA5D4 Series Data Sheet of devices. If you are using one of these devices please read the document located at SAMA5D4 Series Data Sheet.

Notification Status: Final

Description of Change: This revision includes the following changes

Section 3.3 Input/Output Description:	Updated Table 3-3 SAMA5D4 I/O Type Description. Updated Table 3-4 SAMA5D4 I/O Type Assignment and Frequency.
Section 8.2 Peripheral Identifiers	Added Note (2) on SECURAM access in Table 8-1 Peripheral Identifiers.
Section 10. Debug and Test:	Updated Figure 10-1 Debug and Test Block Diagram.
Section 11. Boot Sequence Controller (BSC):	Added address for Boot Sequence Controller Configuration Register.
Section 12. Standard Boot Strategies:	Updated nbSectorPerPage description in section NAND Flash Specific Header Detection (recommended solution).
Section 15. Matrix (H64MX/H32MX):	Added register at 0x280 in Table 15-10 Register Mapping.
Section 28. Parallel Input/Output Controller (PIO):	Updated list of configurable PIOs in Section 28.5.12 Programmable I/O Drive.
Section 29. Multiport DDR-SDRAM Controller (MPDDRC):	Figure 29-1 MPDDRC Module Diagram: updated description. Modified row range in Table 29-8 Interleaved Mapping DDR-SDRAM Configuration Mapping: 8K Rows, 512/1024/2048 Columns, 4 banks.
Section 34. Image Sensor Interface (ISI):	Added important note to Section 34.4.2 Power Management. Added Section 34.5.6 Register Write Protection and added information in relevant registers. Section 34.6.2 ISI Configuration 2 Register: updated RGB_SWAP bit description. Section 34.6.6 ISI Color Space Conversion YCrCb to

	RGB Set 1 Register: updated Yoff, Croff and Cboff bit descriptions. Section 34.6.7 ISI Color Space Conversion RGB to YCrCb Set 0 Register: updated Roff bit description and added Note. Section 34.6.8 ISI Color Space Conversion RGB to YCrCb Set 1 Register: updated Goff bit description and added Note. Section 34.6.9 ISI Color Space Conversion RGB to YCrCb Set 2 Register: updated Boff bit description and added Note. Updated WPVSRC: Write Protection Violation Source description.
Section 39. Serial Peripheral Interface (SPI):	Deleted REQCLR bit in Section 39.8.1 SPI Control Register.
Section 40. Two-wire Interface (TWI):	Updated Figure 40-24 Master Performs a General Call. Updated bit descriptions CHDIV, CLDIV in Section 40.8.5 TWI Clock Waveform Generator Register.
Section 57. Mechanical Characteristics	Added a reference to the Microchip Packaging Specification.
Section 56. Schematic Checklist:	Updated Figure 58-1 1.2V, 1.8V, 2V, 2.5V, 3.3V Power Supplies Schematics (1) for VDDIODDR. Deleted row for Bypass mode in Table 58-2 Clock, Oscillator and PLL Connections.
Section 60. Ordering Information:	Updated Table 60-1 Ordering Information.
Section 61. Errata:	Added: Sections 61.1.10.1, 61.2.10.1: USART Framing error not detected if last data bit is 1 Sections 61.1.12.1, 61.2.12.1: RTC_SR.TDERR flag is stuck at 0

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 09 March 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAMA5D4 Series Data Sheet

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