



## Product Change Notification: SYST-28ITLB269

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**Date:**

01-Nov-2025

**Product Category:**

Ethernet Switches

**Notification Subject:**

Data Sheet - KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface

**Affected CPNs:**

[SYST-28ITLB269\\_Affected\\_CPN\\_11012025.pdf](#)

[SYST-28ITLB269\\_Affected\\_CPN\\_11012025.csv](#)

**Notification Text:**

SYST-28ITLB269

Microchip has released a new Datasheet for the KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface of devices. If you are using one of these devices please read the document located at [KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface](#).

**Notification Status:** Final

**Description of Change:**

DS00002420F (09-12-25)

Throughout document. Updates to grammar and formatting.

Section 6.4.7, "Power-up and Reset Timing", Figure 6-12, Note 1, Figure 6-13:

- Section updated to add an alternate power-up sequence for instances when VDDIO and AVDDH share a power supply.

Table 3-3, "Configuration Strap Descriptions":

- Note for LED2\_1 updated from: "If Port 3 is set to MII or RMII mode, the Speed Select must be 100Mbps Mode." to: "If Port 3 is set to MII or RMII mode, the Speed Select must be 100 Mbps Mode. If the Speed Select is set to 1000 Mbps Mode, Port 3 must be set to RGMII mode."

Table 3-3, "Configuration Strap Descriptions":

- Note for RX\_DV/CRS\_DV/RX\_CTL updated from: "Factory Test Mode is for internal Microchip use only and should not be enabled." to: "Factory Test Mode is for internal Microchip use only and should not be enabled. An external pulldown is required to ensure the switch operates in Normal Mode."

**Impacts to Data Sheet:** See above details.

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 01 Nov 2025

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachments:**

**KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface**

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