Product Change Notification: SYST-26ZZMC491

Date:

28-Aug-2026

Product Category:

Digital Signal Controllers

Notification Subject:

Data Sheet - dsPIC33CK1024MP710 Family Data Sheet

Affected CPNs:

SYST-26ZZMC491_Affected_CPN_08282026.pdf
SYST-26ZZMC491_Affected_CPN_08282026.csv

Notification Text:

SYST-26ZZMC491
Microchip has released a new Datasheet for the dsPIC33CK1024MP710 Family Data Sheet of devices. If you are using one of these devices please read the document located at **dsPIC33CK1024MP710 Family Data Sheet**. **Notification Status:** Final **Description of Change:** This revision incorporates the following updates: • Sections: – Updated Timers/Output Compare/Input Capture, Referenced Sources, 2.4 ICSP Pins, 2.6 External Oscillator Layout Guidance, 3.3 Data Space Addressing, 5.3 Error Correcting Code (ECC), 5.4 ECC Fault Injection, 6. Resets, 6.1.1 Key Resources, 7.1 Interrupt Vector Table, 10.1.1 Source and Destination, 10.1.3 Trigger Source, 10.1.5 Addressing Modes, 10.2.2 DMA Registers, 12.4 PWM4H/L Output on Peripheral Pin Select, 14. High-Speed Analog Comparator with Slope Compensation DAC, 15. Quadrature Encoder Interface (QEI), 21. Timer1, 22.

Capture/Compare/PWM/Timer Modules (SCCP), 22.1 Time Base Generator, 30.9 In-Circuit Debugger and Product Identification System.

– Added 5.6.1 Activating Flash OTP by ICSP Write Inhibit.

• Tables:

– Updated Table 1-1. Pinout I/O Descriptions, Table 7-2. Interrupt Vector Details, Table 10-1. DMA Channel Trigger Sources CHSEL[6:0] Trigger (Interrupt), Table 22-5. Synchronization Sources, Table 33-5. Operating Voltage Specifications, Table 33-6. DC Characteristics: Operating Current (IDD), Table 33-8. DC Characteristics: Power-Down Current (IPD), Table 33-17. I/O Pin Input Injection Current Specifications, Table 33-24. Internal FRC Accuracy, Table 33-32. SPIx Client Mode (Full-Duplex, CKE = 0, CKP =x, SMP = 0) Timing Requirements, Table 33-35. I2Cx Bus Data Timing Requirements (Client Mode), Table 33-37. ADC Module Specifications, Table 34-5. Operating Voltage Specifications and Table 34-6. DC Characteristics: Operating Current (IDD).

– Added Table 33-25. Internal LPRC Accuracy and Table 33-40. Die Temperature Diode Specifications.Registers: – Updated 3.5.12 Data Space Write Page Register, 4.3.4 MBIST Control Register, 5.7.12 ECC System Status Display Register High, 6.1.2 Reset Control Register, 7.7.1 Interrupt Request Flags Register 0, 7.7.2 Interrupt Request Flags Register 1, 7.7.3 Interrupt Request Flags Register 2, 7.7.4 Interrupt Request Flags Register 3, 7.7.5 Interrupt Request Flags Register 4, 7.7.6 Interrupt Request Flags Register 5, 7.7.7 Interrupt Request Flags Register 6, 7.7.8 Interrupt Request Flags Register 7, 7.7.9 Interrupt Request Flags Register 8, 7.7.10 Interrupt Request Flags Register 9, 7.7.11 Interrupt Request Flags Register 10, 7.7.12 Interrupt Request Flags Register 11, 7.7.13 Interrupt Request Flags Register 12, 7.7.21 Interrupt Enable Register 7, 7.7.24 Interrupt Enable Register 10, 7.7.26 Interrupt Enable Register 12, 7.7.46 Interrupt Priority Register 19, 7.7.47 Interrupt Priority Register 20, 7.7.49 Interrupt Priority Register 22, 7.7.55 Interrupt Priority Register 28, 7.7.58 Interrupt Priority Register 31, 7.7.61 Interrupt Priority Register 34, 7.7.63. Interrupt Priority Register 35, 7.7.72. Interrupt Priority Register 46, 7.7.74 Interrupt Priority Register 48, 8.2.2.1 Analog Select for PORTx Register, 8.2.2.2 Output Enable for PORTx Register, 8.2.2.3 Input Data for PORTx Register, 8.2.2.4 Output Data for PORTx Register, 9.11.5 PLL Output Divider Register, 9.11.6 Auxiliary Clock Control Register, 10.2.3.3 DMA Low Address Limit Register, 10.2.3.4 DMA High Address Limit Register, 10.2.3.8 DMA Data Destination Address Pointer Channel n Register, 11.2.1. CAN Control Register Low, 11.2.2. CAN Control Register High, 11.2.3. CAN Nominal Bit Time Configuration Register Low, 11.2.4. CAN Nominal Bit Time Configuration Register High, 11.2.5. CAN Data Bit Time Configuration Register Low, 11.2.6. CAN Data Bit Time Configuration Register High, 11.2.7. CAN Transmitter Delay Compensation Register Low, 11.2.8. CAN Transmitter Delay Compensation Register High, 11.2.9. CAN Time Base Counter Register Low, 11.2.10. CAN Time Base Counter Register High, 11.2.11. CAN Timestamp Control Register Low, 11.2.12. CAN Timestamp Control Register High, 11.2.13. CAN Interrupt Code Register Low, 11.2.14. CAN Interrupt Code Register High, 11.2.15. CAN Interrupt Register Low, 11.2.16. CAN Interrupt Register High, 11.2.17. CAN Receive Interrupt Status Register Low, 11.2.18. CAN Receive Interrupt Status Register High, 11.2.19. CAN Transmit Interrupt Status Register Low, 11.2.20. CAN Transmit Interrupt Status Register High, 11.2.21. CAN Receive Overflow Interrupt Status Register Low, 11.2.22. CAN Receive Overflow Interrupt Status Register High, 11.2.23. CAN Transmit Attempt Interrupt Status Register Low, 11.2.33. CANx Transmit Event FIFO Control Register Low, 11.2.35. CANx Transmit Event FIFO Status Register, 11.2.36. CANx Transmit Event FIFO User Address

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– Removed Interrupt Priority Register 40 and 7.7.1 Interrupt Request Flags Register 0.

– Added DMA High and Low Address Extended Limit Register, DMA Data Source and Destination Extended Address Pointer Channel 0-7 Registers, CRC Data Register Low, CRC Data Register High,CRC Result Register Low, CRC Result Register High,

– Added all PWM Generator x PCI Registers, Auxiliary PWM Generator x PCI Registers and 22.6.6. CCP9 Control 3 Low Register,

• Figures:

– Updated Figure 1. 48-Pin TQFP/VQFN, Figure 2. 64-Pin TQFP, QFN, Figure 3. 80-Pin TQFP, Figure 4. 100-Pin TQFP, Figure 4-6. Data Memory Map for dsPIC33CKXXXXMPXXX Devices,

Figure 7-2. dsPIC33CK1024MP710 Alternate Interrupt Vector Table, Figure 17-4. SPIx Main Connection (Enhanced Buffer Modes), Figure 19-1. PMP Module Pinout and Connections to External Devices and Figure 22-3. Output Compare x Block Diagram.

Impacts to Data Sheet: See above details

Reason for change: To improve productivity

Change Implementation Status: Complete

Date Document Changes Effective: 28 Aug 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33CK1024MP710 Family Data Sheet

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