



Product Change Notification: SYST-25YJXC417

Date:

01-Dec-2025

Product Category:

32-Bit Microprocessors

Notification Subject:

Data Sheet - SAMA5D29 Data Sheet

Affected CPNs:

[SYST-25YJXC417_Affected_CPN_12012025.pdf](#)

[SYST-25YJXC417_Affected_CPN_12012025.csv](#)

Notification Text:

SYST-25YJXC417
Microchip has released a new Datasheet for the SAMA5D29 Data Sheet of devices. If you are using one of these devices please read the document located at SAMA5D29 Data Sheet. Notification Status: Final Description of Change: Section Changes Global Added content related to monetization (ATSAMA5D29-CN(R)-SL3 devices) General format update Reference Document New section Signal Description Table 3-1: updated Timer/Counter rows

Standard Boot Strategies Updated Boot Configuration

Matrix (H64MX/H32MX) MATRIX_PRBSx: corrected MPR field numbering

Special Function Registers (SFR) SFR_OHCIISR: restored RIS1 and RIS2 bits

Shutdown Controller (SHDWC) SHDW_MR: removed AUTOLPM

Real-Time Clock (RTC)

Updated Waveform Generation, Figure 27-8, RTC Accurate Clock Calibration, UTC Mode

RTC_TIMALR (DEFAULT_MODE): updated AMPM description

RTC_MR: updated UTC and HRMODE descriptions

Power Management Controller

(PMC)

Updated Main Crystal Oscillator Failure Detection

Parallel Input/Output Controller

(PIO)

Updated Figure 34-2

Inputs: added Note

PIO_CFGRx: updated DIR description

Static Memory Controller (SMC)

Embedded Characteristics: added ONFI compliance content

Updated SMC Block Diagram, I/O Lines Description

Memory Connection for an 8-bit Data Bus, Memory Connection for a 16-bit Data Bus, Connection of 2 x 8-bit Devices on a 16-bit Bus: Byte Write Option: added note

HSMC_SETUPx, HSMC_PULSEx: corrected register access to “Read/Write”

HSMC_SIGMA0: corrected bitfield name from SIGMA0 to SIGMA

HSMC_SIGMAx: corrected bitfield name from SIGMAx to SIGMA

HSMC_MODEx: removed PS field

DMA Controller (XDMAC) Updated Figure 38-5

Gigabit Ethernet MAC (GMAC)

Embedded Characteristics, Media Access Controller, Jumbo Frames: updated support for jumbo frames

Updated PHY Interface

GMAC_RJFML: updated reset value

GMAC_DCFGR: corrected offset of bit CRCERRREP

GMAC_TQSA: updated bit description

GMAC_NCFGR: updated JFRAME description

USB Device High-Speed Port

(UDPHS)

Updated Transfer Without DMA, Power Management

Flexible Serial Communication

Controller (FLEXCOM)

Updated I/O Lines Description, FIFO Overflow/Underflow Error, FIFO Overflow/Underflow Error, FIFO Overflow/Underflow Error, Baud Rate Generator, Baud Rate in Synchronous Mode or SPI Mode, Baud Rate in Synchronous Mode or SPI Mode

Modified content regarding multiple data reading in SPI Multiple Data Access, FLEX_SPI_RDR (FIFO_MULTI_DATA_8), FLEX_SPI_RDR (FIFO_MULTI_DATA_16)

Index 17 now 'reserved' in: FLEX_TWI_SR (DEFAULT_MODE), FLEX_TWI_SR (FIFO_ENABLED)

FLEX_TWI_SMBTR, FLEX_TWI_SWMR: added detail on WPEN

FLEX_SPI_MR: added LSBHALF

FLEX_US_FESR, FLEX_SPI_SR, FLEX_TWI_FSR: updated TXFPTEF and RXFPTEF definitions

Section Changes

Secure Digital MultiMedia Card

Controller (SDMMC)

Updated Figure 51-4

SDMMC_CA0R: deleted note (2); updated bit descriptions with standard “read-only” mention

SDMMC_CALCR: updated CLKDIV description

Image Sensor Controller (ISC)

Updated White Balance (WB) Module

Rounding, Limiting and Packing (RLP) Module: updated DATY10 table row

ISC_INTEN, ISC_INTDIS, ISC_INTMASK, ISC_INTSR: removed WPE

Controller Area Network (MCAN)

Reworked Timestamping and Timestamp Generation

MCAN_TSCC: updated TSS description

MCAN_TEST: updated RX description

Integrity Check Monitor (ICM) ICM_ISR: updated bit descriptions (cleared on read)

Timer Counter (TC)

Updated Block Diagram

TC_BMR: updated TCxXCxS descriptions

Advanced Encryption Standard

Bridge (AESB)

Register Summary : corrected register order

Advanced Encryption Standard

(AES)

Updated Start Modes, Encrypted Tweak Generation, Data Processing

XEX-based Tweaked-codebook Mode (XTS): updated auto-padding information

Triple Data Encryption Standard

(TDES)

Updated Block Diagram

TC_BMR: updated TCxXCxS descriptions

Analog-to-Digital Controller (ADC)

Updated Table 66-3

ADC_MR: updated reset value

ADC_SEQR2: corrected number of USCH fields (USCH12 is now shown)

Electrical Characteristics

DC Characteristics: added RthJC and RthJB rows in Table 67-2, updated VDDOSC row in Table 67-3

Timing Extraction: updated Figure 67-18

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 01 Dec 2025

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAMA5D29 Data Sheet

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