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Product Change Notification: SYST-24TIVJ982

Date:

01-Oct-2025

Product Category:

Clock Buffers

Notification Subject:

Data Sheet - ZL40272 - Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control

Affected CPNs:

SYST-24TIVJ982_Affected_CPN_10012025.pdf
SYST-24TIVJ982_Affected_CPN_10012025.csv

Notification Text:

SYST-24TIVJ982
Microchip has released a new Datasheet for the ZL40272 - Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control of devices. If you are using one of these devices please read the document located at **ZL40272 - Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control**. **Notification Status:** Final **Description of Change:** Applications: Added information for PCIe Gen 6 and Gen 7 support. Figure 2-23: Added this figure. Table 4-13: Added PCIe Gen 6 & Gen 7 performance values as well as Jitter data for 491.52 MHz clock. Table 4-15: Added PCIe Gen 6 & Gen 7 performance values as well as Jitter data for 491.52 MHz clock.

Impacts to Data Sheet: See above details.

Change Implementation Status: Complete

Date Document Changes Effective: 01 Oct 2025

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

ZL40272 - Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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