Product Change Notification / SYST-22SOSU526

Date:

23-Apr-2021

Product Category:

Computing Embedded Controllers

PCN Type:

Document Change

Notification Subject:

Data Sheet - MEC172x Data Sheet

Affected CPNs:

SYST-22SOSU526_Affected_CPN_04232021.pdf
SYST-22SOSU526_Affected_CPN_04232021.csv

Notification Text:

SYST-22SOSU526

Microchip has released a new Product Documents for the MEC172x Data Sheet of devices. If you are using one of these devices please read the document located at MEC172x Data Sheet.

Notification Status: Final

Description of Change: The updates were made on the following section
1. Table 4-6, "Source Clock Definitions": eSPI frequency updated from "20MHz to 50MHz" to "20MHz to 66MHz.
2. Table 56-3, "DC Electrical Characteristics": Updated ADC VREF input impedance value to 34.5 typical after validation input.
3. Table 33-2, Table 33-3 & Table 33-4: Tables use 24MHz sampling clock, minimum and maximum range of each band is specified in the value mentioned in paren thesis ().
4. Table 57-1, "VTR/VBAT Timing Parameters": Updated VTR and VBAT Rise and Fall time minimum values.
5. Throughout document: External commands removed as external registers are not implemented in device.
6. Document Features: I2C/SMBus Controller bullet: "-1516 Configurable I2C ports" changed to "Up to 16 Configurable I2C ports".
7. Table 2-2, "MEC172x PIN MUX Table": Note for I2C01_SDA and I2C01_SCL removed.
8. Table 42-7, "Typical Flow of a Write Command": Table added.
9. Table 42-8, "Typical Flow of a Read Command": Table added.
10. Section 42.8, "Description" : Example Memory Write Command Sequence and Example Memory Read Command Sequence note added following tables Table 42- 7 and Table 42-8.

11. FIGURE 57-19: SPI Clock Timing on page 765: Updated diagram to add sampling information.
12. FIGURE 57-20: SPI Setup and Hold Times on page 766: Updated diagram to add sampling information.
13. Table 10-5, "Chip-Level (Global) Control/Configuration Registers": OTP ID, Validation ID and Boot ROM Revision ID are Read-Only registering.
14. Table 3-5, "Register Map": Several typos in table corrected.
15. Section 32.0, "Analog Comparator": Analog Comparator chapter added.
16. Table 1-1, "MEC172x Feature List": Optional CACHE controller feature added.
17. 4 Pin JTAG Port List, 2 Pin JTAG Port List and Serial Wire Debug Port List: JTAG Pin information added for clarity.
18. Table 2-4, "Pin Description table": Note 18, Note 19 and Note 20.
19. Table 3-5, "Register Map" : Corrected ARM M4F block (SystemTick, Processor ID, etc) register address. Base address was wrong in the table.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 23 Apr 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

MEC172x Data Sheet

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