



Product Change Notification / SYST-18COSR112

Date:

29-Jan-2024

Product Category:

Microprocessors

PCN Type:

Document Change

Notification Subject:

Data Sheet - SAM9X60 - Ultra-Low Power Arm® ARM926EJ-S™ Processor-Based MPU, 600 MHz, Camera, LCD, 2D Graphics, Dual 10/100 Ethernet, CAN, USB, QSPI, FLEXCOMs, AES, SHA

Affected CPNs:

[SYST-18COSR112_Affected_CPN_01292024.pdf](#)

[SYST-18COSR112_Affected_CPN_01292024.csv](#)

Notification Text:

SYST-18COSR112

Microchip has released a new Datasheet for the SAM9X60 - Ultra-Low Power Arm® ARM926EJ-S™ Processor-Based MPU, 600 MHz, Camera, LCD, 2D Graphics, Dual 10/100 Ethernet, CAN, USB, QSPI, FLEXCOMs, AES, SHA of devices. If you are using one of these devices please read the document located at [SAM9X60 - Ultra-Low Power Arm® ARM926EJ-S™ Processor-Based MPU, 600 MHz, Camera, LCD, 2D Graphics, Dual 10/100 Ethernet, CAN, USB, QSPI, FLEXCOMs, AES, SHA](#).

Notification Status: Final

Description of Change:

Global

Editorial changes throughout

Reference Document

Added.

7. Memories

DDR/SDR I/O Calibration: updated memory types for resistor values.

14. General Purpose Backup Registers (GPBR)

GPBR_FCLR: updated register description.

15. Watchdog Timer (WDT)

WDT_MR: corrected positions of bits WDDBGHLT and WDIDLEHLT.

16. Reset Controller (RSTC)

- RSTC_SR: updated reset value.
17. Real-Time Timer (RTT)
RTT Counting: updated.
RTT_TSR: added TS_OVF bit; increased TSTAMP field width.
18. Real-Time Clock (RTC)
RTC Accurate Clock Calibration: updated.
Waveform Generation: updated.
Waveform Generation for ADC Trigger Event: updated.
RTC_MR: index 1 now 'reserved'. Bit UTC, index 2, updated.
RTC_SR: updated reset value.
Added (DEFAULT_MODE) to register names:
 - 18.6.3. RTC_TIMR (DEFAULT_MODE)
 - 18.6.6. RTC_TIMALR (DEFAULT_MODE)
 - 18.6.8. RTC_CALALR (DEFAULT_MODE)
 - 18.6.16. RTC_TSTR0 (DEFAULT_MODE)
 - 18.6.18. RTC_TSTR1 (DEFAULT_MODE)
 - 18.6.20. RTC_TSDRx (DEFAULT_MODE)
23. OTP Memory Controller (OTPC)
Power Management: updated.
25. Bus Matrix (MATRIX)
No Default Host: updated. Slot Cycle Limit Arbitration: updated.
27. Slow Clock Controller (SCKC)
Switching from Embedded 32 RC Oscillator to 32.768 kHz Crystal Oscillator: modified from 4 to 39000 the number of slow clock cycles to wait for internal resynchronization
29. Power Management Controller (PMC)
32.768 kHz Crystal Oscillator: removed "Reverting to the slow RC oscillator is only possible by shutting down the VDD_NAME power supply."
Main Crystal Oscillator Failure Detection: updated.
CKGR_MOR: corrected reset value.
37. DMA Controller (XDMAC)
Memory to Peripheral Transfer Hierarchy: updated.
41. USB Device High Speed Port (UDPHS)
Transfer Without DMA: modified code content.
Added (DEFAULT_MODE) to register names:
 - UDPHS_EPTCTLENBx
 - UDPHS_EPTCTLDISx
 - UDPHS_EPTCTLx
 - UDPHS_EPTSETSTAx
 - UDPHS_EPTCLRSTAx
 - UDPHS_EPTSTAx
44. Inter-IC Sound Multi-Channel Controller (I2SMCC)
I2S Reception and Transmission Sequence: updated text, figures and tables.
Left-Justified Reception and Transmission Sequence: updated.
I2SMCC_MRB: DMACHUNK description updated. I2SLINESIZE description updated for values 1 and 2.
I2SMCC_ISRA: RXLRDYx and TXRRDYx bit descriptions updated.
46. Flexible Serial Communication Controller (FLEXCOM)
I/O Lines Description: updated.
Baud Rate in Synchronous Mode: updated.
Bus Clear Command, FIFO Pointer Error, FLEX_TWI_CR: modified.
FLEX_TWI_SR (DEFAULT_MODE): updated reset value.
47. Quad Serial Peripheral Interface (QSPI)
QSPI Bus Clock Modes: updated.
48. Secure Digital MultiMedia Card Controller (SDMMC)
SDMMC_CA0R: deleted note (2). Updated bit descriptions with standard "read-only" mention.
SDMMC_CA1R: updated reset value.
49. Image Sensor Interface (ISI)
VSYNC/HSYNC Data Timing: updated.
51. Timer Counter (TC)
Block Diagram: updated. TC_BMR: updated

TCxXCxS descriptions.

55. Triple Data Encryption Standard (TDES)

TDES_MR: updated reset value

56. Random Number Generator (TRNG)

TRNG_WPSR: modified SWETYP description (value 5).

57. Analog-to-Digital Controller (ADC)

ADC_MR: updated reset value.

ADC_PDR: corrected number of channels.

58. Electrical Characteristics

I/O Characteristics: Table 58-13 and Table 58-14: updated with VOL and VOH values.

FLEXCOM TWI Characteristics: updated text and figures.

EMAC Timings: updated EMAC 2 min value.

Low-Power Modes Summary: updated

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 29 Jan 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM9X60 - Ultra-Low Power Arm® ARM926EJ-S™ Processor-Based MPU, 600 MHz, Camera, LCD, 2D Graphics, Dual 10/100 Ethernet, CAN, USB, QSPI, FLEXCOMs, AES, SHA

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