



Product Change Notification: SYST-17PXJE411

Date:

20-Aug-2026

Product Category:

Clock Buffers

Notification Subject:

Data Sheet - ZL40230 - Low Skew, Low Additive Jitter, 10 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output

Affected CPNs:

[SYST-17PXJE411_Affected_CPN_08202026.pdf](#)

[SYST-17PXJE411_Affected_CPN_08202026.csv](#)

Notification Text:

SYST-17PXJE411

Microchip has released a new Datasheet for the ZL40230 - Low Skew, Low Additive Jitter, 10 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output of devices. If you are using one of these devices please read the document located at [ZL40230 - Low Skew, Low Additive Jitter, 10 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output](#).

Notification Status: Final

Description of Change:

Added PCIe Gne 7 to first bullet point under Applications section on first page. Added a new scope image ("491.52 MHz HCSL Phase Noise:") after Figure 3-12, making it the new Figure 3-13. Renumbered the "156.25 MHz LVPECL Phase Noise" scope image from Figure 3-13 to Figure 3-14 and renumbered all following images within the Typical Device Performance Section accordingly. Updated the HCSL outputs for VDDO = 3.3V output frequency maximum value in Table 5-15 from 400 MHz to 800 MHz. Added PCIe 6.0 and PCIe 7.0 additive jitter, additive RMS jitter, and noise floor values to Table 5-15, too. Updated the back matter with most current version.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Aug 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ZL40230 - Low Skew, Low Additive Jitter, 10 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output

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