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16-Bit - Microcontrollers And Digital Signal Controllers

Notification Subject:

Data Sheet - dsPIC33AK128MC106 Family Data Sheet

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Notification Text:

SYST-17HBFC300
Microchip has released a new Datasheet for the dsPIC33AK128MC106 Family Data Sheet of devices. If you are using one of these devices please read the document located at **dsPIC33AK128MC106 Family Data Sheet**. **Notification Status:** Final **Description of Change:** Sections: – Updated Two High-Speed Analog-to-Digital Converters, Peripheral Features, Security Module, Safety Features, Qualification , Programming and Debug Interfaces, Targeted Applications, Pin Diagrams, 3.3.12.2.2 MCU Multiply Instructions, 3.3.12.4 Round Logic, 3.4 Prefetch Branch Unit (PBU), 3.4.1 Architectural Overview, 3.6.2 Architectural Overview, 3.6.2.2 Introduction to Floating Point, 3.6.3.2.2 Flush-To-Zero (FTZ), 3.6.8.1 Floating-Point Unit Registers, 3.6.8.3 FPU Register Set, 4. Memory Organization, 4.1.2.1 Unique Device Identifier (UDID), 4.4.5 Bus Error, 4.4.5.1 Valid Targets, 4.4.6.1 Instruction RAM Window Registers, 5.4.6 Error Correcting Code (ECC), 5.4.6.2 Performing Fault Injection, 7. Configuration Bits, 8. Security Module, 8.6 Peripheral Access Controller (PAC), 9.3.1 System Reset, 9.3.5 Watchdog Time-Out Reset, 9.3.8 Configuration Mismatch Reset (CM), 9.5.1 Special Function Register (SFR) Reset States, 9.5.2 Configuration Word

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– Added 10.9.1.2 Bus Error Trap During Vector Fetch.

– Removed FPU Hazards, FPU Structural Hazards, FPU Data Hazards, Instruction/Hazard Tracker, CPU Write Stalls, FPU Instruction Kill, Register Locking and Unlocking, , Memory Boundary, Ping Pong Transmit Steady State, Ping Pong Transmit Initialization, Ping-Pong Data Receive, Ping Pong Receive Steady State, Ping Pong Receive Initialization,38.1 Package Marking Information and Product Identification System.

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– Added a new Register Bit Attribute Legend table to all registers.

• Registers:

– Updated 3.2.5 Core Mode Control Register, 3.4.2.1 Cache Control Register, 3.4.2.2 Cache Status Register, 3.6.4 Floating-Point Data Register (F0-F31), 3.6.5 Floating-Point Control Register, 3.6.6 Floating-Point Status Register, 3.6.7 Floating-Point Exception Address Capture Register, 4.3.4 BMX Error Status Register for X Data Bus, 4.3.5 BMX Error Status Register for Y Data Bus, 4.3.6 BMX Error Status Register for DMA, 4.3.8 BMX Error Status Register for NVM, 4.3.9 BMX Error Status Register for ICD, 5.3.1 RAM ECC Control Register, 5.3.2 RAM ECC Status Register, 5.3.3 RAM ECC Fault Pointer Register, 5.3.4 RAM ECC Fault Injection Address Register, 5.3.5 RAM ECC Error Address Register, 5.3.6 RAM ECC Error Data Register, 5.3.7 RAM ECC Value Register, , 5.3.8 RAM ECC Syndrome Register,5.3.9 PWB ECC RAM Control Register, 5.3.10 PWB ECC RAM Status Register,5.3.11 PWB ECC RAM Fault Pointer Register, 5.3.12 PWB ECC RAM Fault Injection Address Register, 5.3.13 PWB ECC RAM Error Address Register, 5.3.14 PWB ECC RAM Error Data Register, 5.3.15 PWB ECC RAM Value Register, 5.3.16 PWB ECC Syndrome Register, 6.2.20 NVM CRC Start Address Register, 6.2.21 NVM CRC End Address Register, 7.1.3 FDEVOPT Configuration Register, 7.1.11 FEPUCB Configuration Register, 8.2.2 IRT Control Register, 9.2.1 Reset Control Register, 10.4.10 Interrupt Request Flags Register 1, 10.4.19 Interrupt Enable Register 1, 10.4.45 Interrupt Priority Register 18 through 10.4.57 Interrupt Priority Register 34, 11.3.29 Peripheral Pin Select Input Register 19, 11.3.30 Peripheral Pin Select Input Register 20, 11.3.31 Peripheral Pin Select Input Register 21, 12.3.2 Oscillator Configuration Register, 13.3.5 DMA Channel x Control Register, 13.3.6 DMA Channel x Selection Register, 13.3.7 DMA Channel x Status Register, 13.3.8 DMA Channel x Source Address Register, 13.3.9 DMA Channel x Destination Address Register, 13.3.10 DMA Channel x Count Register, 13.3.11 DMA Channel x Clear Register, 13.3.12 DMA Channel x Set Register, 13.3.13 DMA Channel x Invert Register, 13.3.14 DMA Channel x Mask Register, 15.3.1 ADC n Control Register, 15.3.2 ADC n Test Mode Register, 15.3.3 ADC n Result Ready Status Flags Register, 15.3.5 ADC n Software Trigger Request Register, 15.3.6 ADC 1 Channel x Control Register, 15.3.7 ADC 1 Channel x Data Result Register, 15.3.9 ADC 1 Channel x Compare Low Register, 15.3.10 ADC 1 Channel x Compare High Register, 15.3.12 ADC 2 Channel x Control Register, 15.3.13 ADC 2 Channel x Data Result Register, 15.3.15 ADC 2 Channel x Compare Low Register, 15.3.16 ADC 2 Channel x Compare High Register, 16.3.5 DAC Slope x Control Register, 17.3.1 QEI Control Register, 18.3.2 UARTx Status Register, 18.3.6 UARTx Timing Parameter A Register, 18.3.7 UARTx Timing Parameter B Register, 19.3.1 SPIx Control Register 1, 19.3.4 SPI Buffer Register, 19.3.5 SPIx Baud Rate Generator Register, 21.3.1

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– Removed Peripheral Pin Select Input Register 4 (RPINR4), Peripheral Pin Select Output Register 3 (RPOR3), Peripheral Pin Select Output Register 7 (RPOR7), Peripheral Pin Select Output Register 11 (RPOR11)

• Figures

– Updated Figure 1-1. dsPIC33AK128MC106 Family Block Diagram, Figure 2-1. Recommended Minimum Connection, Figure 3-1. dsPIC33A Core Conceptual Block Diagram with FPU Coprocessor, Figure 3-9. DSP Engine Block Diagram, Figure 3-10. Integer and Fractional Representation of 0x40000001, Figure 3-11. Integer and Fractional Representation of 0xC0000002, Figure 8-2. PAC Locking Behavior, Figure 13-2. DMA Channel Controllers Block Diagram, Figure 13-3. Types of DMA Data Transfers, Figure 13-4. Common Logic Flow for Data Transfer Modes, Figure 13-5. Null Write Mode, Figure 13-6. Ping-Pong Support Connection, Figure 13-7. Ping-Pong – Transmit, Figure 15-1. ADC Module Block Diagram, Figure 18-3. UART Clocking Diagram, Figure 18-4. Fractional Division Mode, Figure 19-8. SPIx Host/Client Connection Diagram, Figure 19-12. SPIx Host, Frame Host Connection Diagram, Figure 23-1. Timer1 Block Diagram, Figure 29-1. Basic Op Amp Block Diagram and Figure 30-1. Watchdog Timer Block Diagram.

– Removed Timer1 Clock Input Logic

• Examples: – Updated Example 10-3. ISR for Timer 1 Interrupt, Example 12-1, Example 12-3. Code Example for Using PLL with the Primary Oscillator (POSC), Example 12-4. Code Example for Using PLL with 8 MHz Internal FRC, Example 13-3. Typical Code Sequence for a Continuous Transfer, Example 13-4. Typical Code Sequence for a Repeated Continuous Transfer, Example 13-5. Code for Fixed to Block Continuous Transfer (Peripheral to Memory), Example 13-6. Null-Write Mode, Example 15-3. Gain Error Calibration Example, Example 15-4. Single Conversion Example, Example 15-5. Windowed Conversions Example, Example 15-6. Integration of the Multiple Samples Example, Example 15-7. Oversampling Example, Example 15-8. Comparator Example, Example 15-9. Multiple Channels Scan Example, Example 15-10. Second Order Low Pass Filter Example,Example 16-4. Initialize DAC with Slope Compensation, Example 16-5. DAC Settings for Hysteretic Mode, Example 18-1. UART1 Transmission with Interrupts, Example 18-2. UART1 Reception with Interrupts, Example 18-3. Address Detect Transmission, Example 18-4. Address Detect Reception, Example 19-1. Initialization Code for 16-Bit SPI Host Mode, Example 21-2. SENT1 Asynchronous Transmission Code, Example 21-3. SENT1 Synchronous Transmission Code, Example 21-4. SENT1 Reception Code, Example 21-5. SENT Transmission (SPC Pulse Reception), Example 21-6. SENT Reception (SPC Pulse Transmission), Example 24-1. Setup for Input Capture mode (Every Rising Edge)Example 26-6. Interleaved Sampling Step Command Program, Example 26-7. Ratioed Sampling Step Command Program, Example 28-2. Single-Ended Positive Voltage Shift with 50 µA Selection and Example 30-3. WDT Configuration

Example.

– Added Example 5-1. Program Execution from RAM,

• Equations:

• – Updated Equation 18-1. Baud Rate When BRG = 0, Equation 18-3. Baud Rate Formulas, Equation 19-1. SCKx Frequency, Equation 19-2. Baud Rate Calculation, Equation 20-1. BRG Reload Value Calculation and Equation 21-1. Tick Period Calculation, – Added Equation 12-1. FRACDIV,

Minor grammatical corrections and formatting changes throughout the document.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Mar 2025

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33AK128MC106 Family Data Sheet

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