Product Change Notification: SYST-11QRTJ113

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17-Jul-2026

Product Category:

Digital Signal Controllers

Notification Subject:

Data Sheet - dsPIC33AK512MPS512 Family Data Sheet

Affected CPNs:

SYST-11QRTJ113_Affected_CPN_07172026.pdf
SYST-11QRTJ113_Affected_CPN_07172026.csv

Notification Text:

SYST-11QRTJ113
Microchip has released a new Datasheet for the dsPIC33AK512MPS512 Family Data Sheet of devices. If you are using one of these devices please read the document located at **dsPIC33AK512MPS512 Family Data Sheet**. **Notification Status:** Final **Description of Change:** Revision D (July 2026) Sections: Updated High-Performance dsPIC33A DSP CPU, High-Resolution PWM, Analog Features, Qualification, Programming and Debug Interfaces, 2.2. Decoupling Capacitors, 5. Data Memory, 6.4.3.4. Inactive Panel Erase, 8.6.3. Operations, 8.6.3.3. Operations in Sleep/Idle Modes, 10.6.5. INTTREG, 11.4.11.2.7. Self-Test, 11.8. Interrupt Sequence, 12.4.4. Internal Fast RC (FRC) Oscillator, 12.4.5. BFRC Oscillator, 12.4.6. Phase-Locked Loop (PLL), 12.4.6.3.1. Setup for Using PLL with the Primary Oscillator (POSC), 15.5.2.2.1. Independent Edge PWM Mode, 15.5.9.3.2. Frequency Scaling, 16. 40 MSPS Analog-to-Digital Converter (ADC), 16.4.13. Calibration, 16.4.13.1.1. Error Compensation Coefficient Calculation, 18.1. Device-Specific Information,

21.4.1.5.1. Host Mode Operation, I2S Audio Client Mode of Operation, 32-Bit Operation with Single Compare Mode and 44. Product Identification System.

Tables:

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Module Specification, Table 41-16. ADC Module Specifications and Table 41-17. Operational Amplifier Specifications.

Added Op Amp Calibration Register Description, I/O Pin Input Injection Current Specifications, DC Characteristics: Watchdog Timer Delta Current (ΔIWDT) and DC Characteristics: CLKGEN Delta Current.

Removed Table 16-2. ADC Clock Source Select bit (CLKSEL bits in ADxCON2 Register) and Table 17-2. ADC Clock Source Select bit (CKSEL bits in ADCxCON2 Register).

Registers:

Updated 3.2.3. REPEAT Loop Counter Register, 3.2.5. Core Mode Control Register, 3.2.6. Modulo Addressing Control Register, 3.2.7. X AGU Modulo Addressing Start Register, 3.2.8. X AGU Modulo Addressing End Register, 4.2.9. Y AGU Modulo Addressing Start Address Register, 3.2.10. Y AGU Modulo Addressing End Register, 3.2.13. Force Execution Instruction Register 1, 3.2.14. Force Execution Instruction Register 2, 3.2.15. Debug Hold PC Register, 3.2.16. Vector Fail Address Register, 3.4.2.1. Cache Control Register, 3.4.2.2. Cache Status Register, 3.4.2.3. Cache Fault Injection Register, 3.5.2.1. HPCCON Register, 3.5.2.2. HPCSEL0 Register, 3.5.2.3. HPCSEL1 Register, 3.5.2.4. HPCCNTLx Register, 3.5.2.5. HPCCNTHx Register, 3.6.6. Floating-Point Status Register, 4.3.1. Bus Initiator Priority Control Register, 4.3.2. BMX Instruction RAM Low Address Register, 4.3.3. BMX Instruction RAM High Address Register, 4.3.4. BMX Error Status Register for X Data Bus Initiator, 4.3.5. BMX Error Status Register for Y Data Bus Initiator, 4.3.6. BMX Error Status Register for DMA Initiator, 4.3.7. BMX Error Status Register for CPU Initiator, 4.3.8. BMX Error Status Register for Crypto Module Initiator, 4.3.9. BMX Error Status Register for CAN 1 Initiator, 4.3.10. BMX Error Status Register for CAN 2 Initiator, 4.3.11. BMX Error Status Register for Program Space Initiator, 4.3.12. BMX Error Status Register for Debug Initiator, 5.4.3.4. MBIST Control Register, 6.2.1. Nonvolatile Memory (NVM) Control Register, 6.2.2. Nonvolatile Memory Lower Address Register, 6.2.7. NVM Source Data Address Register, 7.2.8. NVM ECC Control Register, 6.2.9. ECC RAM Status Register, 6.2.10. NVM ECC Fault Injection Pointer Register, 6.2.11. NVM ECC Fault Injection Address Register, 6.2.12. NVM ECC Error Address Register, 6.2.13. NVM ECC Error Data 0 Register, 6.2.15. NVM ECC Error Data 2 Register, 6.2.17. NVM ECC Value Register, 6.2.16. NVM ECC Error Data Register, 6.2.17. NVM ECC Value Register, 6.2.18. NVM ECC Syndrome Register, 6.2.19. NVM CRC Control Register, 6.2.20. NVM CRC Start Address Register, 6.2.21. CRC End Address Register, 6.2.22. NVM CRC Seed Register, 6.2.23. NVM CRC Output Data Register, 7.1.6. FPRxST Configuration Register, 7.1.7. FPRxEND Configuration Register, 7.1.11. FEPUCB Configuration Register, 7.1.12. FWPUCB Configuration Register, 7.1.13. FBOOT Configuration Register, 8.2.2. IRT Control Register, 8.2.4. Protection Region n Control Register, 8.2.5. Protection Region n Start Address Offset Register, 8.2.6. Protection Region n End Address Offset Register, 8.2.8. Peripheral Access Control Register 1, 8.2.9. Peripheral Access Control Register 2, 8.2.10. Peripheral Access Control Register 3, 8.6.2.1. Crypto Accelerator Enable Register, 10.4.5. Interrupt Control Register 5, 10.4.6. Interrupt Control and Status Register, 10.4.9. Interrupt Request Flags Register 0, 10.4.11. Interrupt Request Flags Register 2, 10.4.21. Interrupt Enable Register 0, 10.4.23. Interrupt Enable Register 2, 10.4.29. Interrupt Enable Register 8, 10.4.30. Interrupt Enable Register 9, 10.4.34. Interrupt Priority Register 0, 10.4.35. Interrupt Priority Register 1, 10.4.37. Interrupt Priority Register 3, 10.4.41. Interrupt Priority Register 8, 10.4.42. Interrupt Priority Register 9, 10.4.69. Interrupt Priority Register 42, 11.3.23. Peripheral Pin Select

Input Register 9, 11.3.24. Peripheral Pin Select Input Register 10, 11.3.25. Peripheral Pin Select Input Register 11, 11.3.26. Peripheral Pin Select Input Register 12, 11.3.62. Peripheral Pin Select Output Register 21, 11.3.68. Peripheral Pin Select Output Register 32, 11.3.69. Peripheral Pin Select Output Register 33, 11.3.70. Peripheral Pin Select Output Register 34, 11.3.71. Peripheral Pin Select Output Register 35, 11.3.72. IOIM x Control Register, 12.3.2. Oscillator Configuration Register, 12.3.3. Reference Clock Fail Status Register, 12.3.4. Source Clock Selection Fail Status Register, 12.3.5. Clock Generator Control Register, 12.3.6. Clock Generator Divider Register, 12.3.10. PLL Control Register, 12.3.11. PLL Divider Register, 12.3.16. Clock Monitor Prescaler Register, 12.3.17. Clock Monitor Input Selection Register, 12.3.18. Clock Monitor Buffer Register, 12.3.19. Clock Monitor Saturation Register, 12.3.20. Clock Monitor High Threshold Failing Register, 12.3.21. Clock Monitor Low Threshold Failing Register, 12.3.23. Clock Monitor Low Threshold Warning Register, 13.3.2. DMA Data Buffer Register, 13.3.22. Clock Monitor High Threshold Warning Register, 13.3.10. DMA Channel x Count Register, 14.4.1. CAN FD x Control Register, 14.4.15. CAN Bus Diagnostics Register 0, 14.4.16. CAN Bus Diagnostics Register 1, 15.3.7. ADC n Channel 0 Control Register 1, 15.3.9. ADC n Channel 0 Data Register, 15.3.10. ADC 1 Channel n Result Register, 15.3.18. ADC n Channel 1 Counter Register, 15.3.25. ADC 1 Channel n Counter Register, 15.4.1. PWM Clock Control Register, 15.4.3. Frequency Scaling Minimum Period Register, 15.4.5. Master Duty Cycle Register, 15.4.11. PWM Generator x Control Register, 15.4.12. PWM Generator x Status Register, 15.4.14. PWM Generator x I/O Control 2 Register, 15.4.24. PWM Generator x FF PCI 2 Register, 15.4.25. PWM Generator x SP PCI 1 Register, 15.4.30. PWM Generator x Duty Cycle Adjustment Register, 15.4.40. Auxiliary PWM Clock Control Register, 15.4.43. Auxiliary PWM Master Phase Register, 15.4.44. Auxiliary PWM Master Duty Cycle Register, 15.4.45. Auxiliary PWM Master Period Register, 15.4.47. Auxiliary PWM Combinational Trigger Register, 16.4.78. Auxiliary PWM Generator x Capture Register, 16.3.1. ADC n Control Register, 16.3.5. ADC n Comparators Status Register, 16.3.6. ADC n Software Triggers Request Register, 17.2.1.1. ITC Control Register 1, 17.2.1.2. Control Register 2, 17.2.1.3. ITC Status Register, 17.2.1.7. Comparator Hit Register, 17.2.1.8. List x Control Register, 17.2.1.9. List x Status Register, 17.2.1.13. ITC List x Acquisition and Post-Processing Control Register, 17.2.1.15. Records Pair Configuration Register, 17.2.1.16. Record x Result Register, 17.2.1.17. Current Result Register, 17.2.1.18. ITC Acquisition Sequence Commands Word x Register, 17.2.1.20. Acquisition Sequence Commands Array Map Register, 17.2.1.21. Math Sequence Commands Array Map Register, 18.3.2. DAC Control 2 Register, 18.3.3. DAC Control Register, 18.3.4. DACx Control Low Register, 19.3.7. Position Counter x Hold Register, 20.3.6. UARTx Timing Parameter A Register, 21.3.3. SPIx Status Register, 20.3.4. UARTx Receive Buffer Register, 21.3.1. SPIx Control Register 1, 22.3.3. SPIx Status Register, 21.3.4. SPI Buffer Register, 21.3.5. SPIx Baud Rate Generator Register, 22.4.6. I2Cx Transmit Data Register, 22.4.7. I2Cx Receive Data Register, 23.3.6. SENTx Data Register, 23.4.18. I2C Host Input Delay Compensation Register, 24.3.6. BiSS Control Communication Configuration Register, 25.3.1. Timer x Control Register, 25.3.3. Period Register 1, 25.3.9. BiSS Communication Status Register, 25.3.12. BiSS Configuration Register, 26.3.2. CCPx Control Register 2, 26.3.4. CCPx Status Register, 26.3.6. CCPx Period Register, 27.3.1. Configurable Logic Cell x Control Register, 28.3.1. PTG Control Register, 29.2.1. CRC Control Register, 29.2.2. CRC XOR Register, 29.2.3. CRC Data Register, 30.3. Current Bias Generator Control Register, 31.2. UREF Control Register 1, 35.2.3. Peripheral Module Disable 2 Register, 35.2.4. Peripheral Module Disable 3 Register and 35.2.5. Peripheral Module Disable 4 Register.

Updated all ADC registers to properly show 5 ADC instances and 16 ADC channels.

Added 10.4.62. Interrupt Priority Register 29, 10.4.63. Interrupt Priority Register 30 and 10.4.64. Interrupt Priority Register 31.

Figures:

Updated Figure 1-1. dsPIC33AK512MPS512 Family Block Diagram, Figure 4-1. Memory Map for dsPIC33AK512MPS512, Figure 10-4. Interrupt Latency, Figure 11-5. IOIM Block Diagram, Figure 13-14. Monitor Function, Figure 14-48. Interrupt Multiplexing, Figure 15-4. PWM Generator Clocking and Figure 18-1. High-Speed Analog Comparator Module Block Diagram.

Examples:

Updated Example 13-3. Code Example for Using PLL with the Primary Oscillator (POSC), Example 16-3. Gain Error Calibration Example and Example 33-3. WDT Configuration Example.

Equations:

Updated Equation 16-2. Two Reference Voltages Gain Error Compensation Coefficient and Offset Error Calculation.

Minor grammatical corrections and formatting changes have been made throughout the document.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33AK512MPS512 Family Data Sheet

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