Product Change Notification: SYST-11MPWT773

Date:

19-Aug-2026

Product Category:

32-Bit Microprocessors

Notification Subject:

Data Sheet - SAM9X7 Series Data Sheet

Affected CPNs:

SYST-11MPWT773_Affected_CPN_08192026.pdf
SYST-11MPWT773_Affected_CPN_08192026.csv

Notification Text:

SYST-11MPWT773
Microchip has released a new Datasheet for the SAM9X7 Series Data Sheet of devices. If you are using one of these devices please read the document located at **SAM9X7 Series Data Sheet**. **Notification Status:** Final **Description of Change:** Product Identification System Updated example Microchip Recommended Power Management Solutions Updated Figure 9.1 and Figure 9.2 Memory Mapping Figure 11.1: corrected SYSCWP offset Peripheral Identifiers Table 12.1: restored GMAC (ID 67) row; updated PMECC (ID 48) row Memories Updated Clocks

Static Memory Controller (SMC)

Updated Figure 20.1

SMC_OCMS: corrected field name to CSxSE

Programmable Multibit ECC

Error Location Controller

(PMERRLOC)

PMERRLOC_SIGMA0: renamed field from SIGMA0 to SIGMA

PMERRLOC_SIGMAx: renamed field from SIGMAx to SIGMA

Real-Time Clock (RTC)

Updated UTC Mode

Updated RTC_TSTRx, RTC_TSDRx, RTC_TSSRx register descriptions

RTC_MR: updated UTC and HRMODE descriptions

RTC_TIMALR (DEFAULT_MODE): updated AMPM description

Debug Unit (DBGU) Updated Chip Identifier and DBGU_CIDR

Special Function Registers (SFR) SFR_TSU_CFG: updated WIDTH description

Power Management Controller

(PMC)

Updated Spread Spectrum

Parallel Input/Output Controller

(PIO)

PIO_ABCDSR1 and PIO_ABCDSR2 renamed PIO_ABCDSR0 and PIO_ABCDSR1

PIO_DRIVER1 renamed PIO_DRIVER

Analog-to-Digital Controller

(ADC)

Added ADC Input Sampling Capacitor Charging Time (Tracking Time), Maximum Sampling Frequency

Analog-to-Digital Conversion: updated tracking time information

ADC_MR: updated TRACKTIM description

ADC_ACR: corrected reset value; updated IBCTL description

ADC_EMR: updated TRACKX4 description

LCD Controller (LCDC)

Split the LCDC_LCDCFG5 register into LCDC_LCDCFG5 (DEFAULT_MODE) and LCDC_LCDCFG5 (DPICOMPLIANT_

MODE)

2D Graphics Engine (GFX2D) BLEND_WD5: updated SPRE and DPRE descriptions

Display Serial Interface (DSI)

High-Speed Frequency Range Control Operation: updated Table 49.3

D-PHY PLL Control Operation: updated Table 49.4
Section Changes

Camera Serial Interface (CSI)

Added Data ID Monitors

Added the following registers:

• CSI_DATA_IDS_1

• CSI_DATA_IDS_VC_1

• CSI_DATA_IDS_VC_2

• CSI_VC_EXTENSION

• CSI_INT_ST_LINE

• CSI_INT_MSK_LINE

• CSI_INT_FORCE_LINE

• CSI_INT_ST_BNDRY_FRAME_FATAL

- CSI_INT_MSK_BNDRY_FRAME_FATAL
- CSI_INT_FORCE_BNDRY_FRAME_FATAL
- CSI_INT_ST_SEQ_FRAME_FATAL
- CSI_INT_MSK_SEQ_FRAME_FATAL
- CSI_INT_FORCE_SEQ_FRAME_FATAL
- CSI_INT_ST_CRC_FRAME_FATAL
- CSI_INT_MSK_CRC_FRAME_FATAL
- CSI_INT_FORCE_CRC_FRAME_FATAL
- CSI_INT_ST_PLD_CRC_FATAL
- CSI_INT_MSK_PLD_CRC_FATAL
- CSI_INT_FORCE_PLD_CRC_FATAL
- CSI_INT_ST_DATA_ID
- CSI_INT_MSK_DATA_ID
- CSI_INT_FORCE_DATA_ID
- CSI_INT_ST_ECC_CORRECT
- CSI_INT_MSK_ECC_CORRECT
- CSI_INT_FORCE_ECC_CORRECT

Updated CSI_INT_ST_MAIN

CSI_SCRAMBLING_SEED3: corrected reset value

Image Sensor Controller (ISC) Embedded Characteristics: updated Parallel Interface characteristic

Inter-IC Sound Multi-Channel

Controller (I2SMCC)

Updated Monitors and Reports

DMA Controller Operation: added Table 55.4 and Table 55.5

I2SMCC_MRB: updated DMACHUNK description

I2SMCC_IERA, I2SMCC_IDRA, I2SMCC_IMRA, I2SMCC_ISRA: removed bits with indexes greater than 0

Advanced Encryption Standard

(AES)

Updated Start Modes, Encrypted Tweak Generation, Data Processing

XEX-based Tweaked-codebook Mode (XTS): updated auto-padding information

Secure Hash Algorithm (SHA)

Updated Description, SHA Algorithm, Protocol Layers Improved Performances

SHA_WPMR: updated ACTION description

SHA_CR: updated SWRST description

SHA_MR: corrected ALGO description

SHA_ISR: corrected URAT description

Triple Data Encryption Standard

(TDES)

Updated Security and Safety Analysis and Reports

TDES_MR: modified PKRS description
Section Changes

Ethernet MAC (GMAC)

Updated 1588 Timestamp Unit

Table 64.2: updated field 12:0

GMAC_MAN: updated OP description

GMAC_TSCTL: corrected field name from TXSQ0 to TXSQ

Flexible Serial Communication

Controller (FLEXCOM)

Modified content regarding multiple data reading in SPI Multiple Data Access, FLEX_SPI_RDR

(FIFO_MULTI_DATA_8), FLEX_SPI_RDR (FIFO_MULTI_DATA_16)

Updated Table 65.2

FLEX_SPI_RDR (FIFO_MULTI_DATA_8), FLEX_SPI_RDR (FIFO_MULTI_DATA_16), FLEX_SPI_TDR

(FIFO_MULTI_DATA): “FIFO” removed from register name (but kept in register acronym)

Quad Serial Peripheral Interface

(QSPI)

Updated Scrambling/Unscrambling Function, Data Strobe Delay Management

Secure Digital MultiMedia Card

Controller (SDMMC)

Split the SDMMC SDMA System Address/Argument 2 Register into SDMMC_SSAR (DEFAULT_MODE)

and SDMMC_SSAR (CMD23)

USB Device High Speed Port

(UDPHS)

Updated Power Management

Added Detach Procedure (Software Disconnect)

Transfer Without DMA: updated “Important” note

Register Summary: corrected format of registers suffixed with “(DEFAULT_MODE)”

UDPHS_CTRL: updated DETACH description

UDPHS_TST: updated SPEED_CFG description

USB Host High Speed Port

(UHPHS)

Updated Figure 73.2

Electrical Characteristics

12-bit ADC Characteristics: added table footnote (1)

Updated Table 74.50, Table 74.67, Flexible Serial Communication Controller (FLEXCOM) - USART

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 19 Aug 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM9X7 Series Data Sheet

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