Product Change Notification: SYST-11HBHM253

Date:

17-Jul-2026

Product Category:

Digital Signal Controllers

Notification Subject:

Data Sheet - dsPIC33AK256MPS306 Family Data Sheet

Affected CPNs:

SYST-11HBHM253_Affected_CPN_07172026.pdf
SYST-11HBHM253_Affected_CPN_07172026.csv

Notification Text:

SYST-11HBHM253

Microchip has released a new Datasheet for the dsPIC33AK256MPS306 Family Data Sheet of devices. If you are using one of these devices please read the document located at **dsPIC33AK256MPS306 Family Data Sheet**.

Notification Status: Final

Description of Change:

This revision incorporates the following updates.

Sections: Updated Operating Conditions, High-Speed Analog-to-Digital Converters, Controller Features, Security Features, Analog Features, Qualification, Vendor Specific Directed Read CCC's, 3.3.18.3.1. Bit-Reversed Addressing Implementation, 3.6.3.2. Subnormal Number, 5.4.3.1. BIST at Start-up, 8. Security Module, 8.6.3. Operations, 8.6.3.3. Operations in Sleep/Idle Modes, 9.4.7.2. Device Reset Request, 11.4.6. Considerations for Peripheral Pin Selection, 13.4.7.1. Common Transfer Mode Sequence, 13.4.8.2. Fixed to Block, 13.5.1.2. Transfer Size, 13.5.2. Source Descriptor Table (SDT), 13.5.3. Destination Descriptor Table (DDT), 14.7.13. Transmit State Diagram, 15.2. High-Resolution Mode (Fine Edge Placement), 15.4.2. Frequency Scale Register, 15.4.7. Linear Feedback Shift Register, 15.4.10. PWM Event Output Control Register y, 15.4.12. PWM Generator x Status Register, 15.4.17. PWM Generator x F1 PCI 1 Register, 15.4.25. PWM Generator x SP PCI 1

Register, 16.4.1. Channels, 16.4.4. Conversions, 16.5. 16-bit Resolution Mode, 17.4.16. Acquisition Sequencer Commands, 17.4.18. Hardware Coded Sequences, 17.5.1. CVD Scan of Three Analog Inputs Using a Hardcoded Processing Sequence, 17.5.2. CVD Scan of All Analog Inputs Using a Custom Processing Sequence Defined in Software, 24.4.4.1. SCL Generation and Timings, 24.4.5.1.3. Handling the GETSTATUS CCC, 24.4.5.1.4. Handling ENTDAA, GETPID and GETDCR, Vendor Specific Write CCCs, Vendor Specific Directed Read CCC's, 24.4.5.2.1. Handling Private Receive (Controller Write) Transfers, 24.4.5.2.2. Handling Private Transmit (Controller Read) Transfers, Target Interrupt Request Generation with Virtual Target, 24.4.5.3. Hot-Join Request, 24.4.5.4. Target Interrupt Request Generation, 24.4.5.5. Controller Request Generation, Detecting Dead Bus, Recovery Sequence, and 24.4.5.6.2. Extended Response Data Structure, 25.4.2.2. Receiver Status, 26.5.4. Broadcast Command Code Example, 27.4.2. Synchronous External Clock Counter Mode, 27.4.3. Gated Timer Mode, 27.4.3.2. Gated Timer Initialization Steps, 27.4.7. Asynchronous External Clock Counter Initialization Steps, 27.4.8. Timer Prescalers, 27.4.9. Writing to TxCON, TMRx and PRx Registers, and 28.4.4.4.6. Output Polarity Control. High-Temperature Electrical Characteristics was added.

Registers: Updated 3.2.13. Force Execution Instruction Register 1, 3.2.14. Force Execution Instruction Register 2, 3.2.16. Vector Fail Address Register, 3.4.2.3. Cache Fault Injection Register, 3.4.2.5. Cache RAM Command Register (Address/Control), 3.4.2.6. Tag Data Register, 3.4.4.5.1. Buffer Slice Architecture, 3.5.2.2. HPCSEL0 Register, 3.5.2.3. HPCSEL1 Register, 6.2.1. Nonvolatile Memory (NVM) Control Register, 6.2.11. NVM ECC Fault Injection Address Register, 6.2.12. NVM ECC Error Address Register, 6.2.14. NVM ECC Error Data 1 Register, 6.2.19. NVM CRC Control Register, 6.2.20. NVM CRC Start Address Register, 6.2.21. NVM CRC End Address Register, 6.3.3. Error Correcting Code (ECC), 6.4.3.4.1. Inactive Panel Erase Sequence, 7.1.2. FICD Configuration Register, 7.1.3. FDEVOPT Configuration Register, 7.1.4. FWDT Configuration Register, 7.1.6. FPRxCTRL Configuration Register, 7.1.7. FPRxST Configuration Register, 7.1.13. FWPUCB Configuration Register, 7.2.2. Device ID Register, 8.2.5. Protection Region n Start Address Offset Register, 8.2.9. Peripheral Access Control Register 2, 8.6.2.1. Crypto Accelerator Enable Register, 9.1.1. Reset Control Register, 10.4.1. Interrupt Control Register 1, 10.4.3. Interrupt Control Register 3, 10.4.4. Interrupt Control Register 4, 10.4.7. Interrupt Vector Base Address Register, 10.4.9. Interrupt Request Flags Register 0 through 10.4.19. Interrupt Request Flags Register 11, 10.4.20. Interrupt Enable Register 0 through 10.4.30. Interrupt Enable Register 11, multiple Interrupt Priority Registers, 11.3.1. Input Data Register, 11.3.5. Interrupt Change Notification Flag for Register, 11.3.6. Analog Select Register, multiple Peripheral Pin Select and IOIM registers, Clock Generator and PLL registers, DMA, CAN, PWM, ADC, ITC, RDC, DAC, QEI, UART, SPI, I2C, I3C, BiSS, CCP, CLC, CRC, UREF, Deadman Timer, Reset Control, and Peripheral Module Disable registers. All ADC registers were also updated to properly show 3 ADC instances and 12 ADC channels.

Tables: Updated Table 1. dsPIC33AK256MPS306 Family Device Features, Table 4. 64-Pin VQFN, TQFP Complete Pin Function Descriptions, Table 5. Pinout I/O Descriptions, Table 3-19. FP Instruction Exception Conditions, Table 4-1. UDID Address, Table 5-1. Data Memory, Table 6-1. Device Memory Attributes, Table 9-1. Reset Flag Bit Operation, Table 9-4. Status Bits, Their Significance and the Initialization Condition for RCON Register, Table 10-1. Interrupt Vector Details, Table 11-2. PORTB Availability, Table 11-4. PORTD Availability, Table 11-5. ANSELA Availability, Table 11-10. Selectable Input Sources (Maps Input to Function), Table 11-11. Pin Correlation to Input Remap #, Table 11-13. Output Selection for Remappable Pins (RPn), Table 11-17. IOIM Test Conditions, Table 12-3. Clock Generator Clock Resources, Table 12-4. PLL Clock

Sources, Table 12-5. Clock Monitor Clock Resources, Table 13-7. RELOADS/RELOADD/RELOADC Bits and Data Transfer Modes, Table 13-15. Descriptor-Based Operational Sequence, Table 15-1. PWM Summary Table, Table 16-2. ADC Input Availability, Table 16-3. TRGnSRC Trigger Source Selection Bits Value Description, Table 20-4. PIMOD Supports in Varies Mode, Table 22-1. SPI Summary Table, Table 22-7. Sample SCKx Frequencies, Table 24-17. Supported CCC Transfers, Table 24-23. CRHDLY Byte Format, Table 24-27. Extended Transmit Command Data Structure, Table 24-30. Extended Transmit Command Data Structure, 28.4.3.1.2. Timer Clock Source Selection, Table 42-2. Operating MHz vs. Voltage, Table 24-3. Transfer Command Data Structure, Table 25-1. SENT Summary Table, Table 29-4. DS3 Data Selection MUX 3 Signal Selection Bits, Table 30-3. PTG Output Descriptions, Table 42-12. DC Characteristics: PLL Delta Current, Table 42-15. Op Amp Delta Current, Table 42-18. I/O Pin Input Injection Current Specifications, Table 42-25. Internal FRC Accuracy, Table 42-27. Reset and Watchdog Timer Timing Requirements, Table 42-31. SPIx Host Mode (Half-Duplex, Transmit Only) Timing Requirements, Table 42-34. SPIx Client Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 0) Timing Requirements, Table 42-36. I2Cx Bus Data Timing Requirements (Host Mode), Table 42-40. ADC Module Specifications, Table 42-41. ADC Module Specifications, Table 42-42. Die Temperature Diode Specifications, Table 42-45. DACx Output (DACOUTx Pins) Specifications, Table 42-47. Operational Amplifier Specifications, Table 43-2. Operating MHz vs. Voltage, Table 43-4. DC Characteristics: Operating Current (IDD), and Table 43-5. Idle Current (IIDLE). Table 42-18. I/O Pin Input Injection Current Specifications was added, and Table 14-2. CLKSEL Clock Selection bit was removed.

Figures: Updated Figure 11-5. IOIM Block Diagram, Figure 14-14. Message Memory Organization, Figure 14-48. Interrupt Multiplexing, Figure 24-10. Programming Flow to Switch from Controller to Target Mode, Figure 24-36. Vendor Specific Transmit Transfer, Figure 24-41. Flow Diagram for Target Interrupt Request (SIR) Generation, and Figure 27-1. Timer Block Diagram.

Examples: Updated Example 6-3. CRC Checksum Calculation, Example 11-1. Configuring UART1 Input and Output Functions, Example 11-2. Virtual PPS Connection, Example 12-2. Code Example for Using PLL with the Primary Oscillator (POSC), Example 12-3. Code Example for Using PLL with 8 MHz Internal FRC, Example 12-4. Frequency Measurement Function, Example 13-5. Code for Fixed to Block Continuous Transfer (Peripheral to Memory), Example 13-6. Null Write Mode, Example 14-3. Message Reception Code, Example 17-1. ADC 3 Initialization and ITC Enable Code, Example 24-2. Target Mode: After Dynamic Address is Assigned, Perform Private Read and Write, Example 28-2. Setup for Dual Edge Buffered Compare Mode, Example 30-2. PTGCTRL Options, Example 31-2. Calculating the Non-Direct Initial Value (MOD bit = 0), Example 31-3. Routine to Get the Final CRC Result in Legacy Mode (MOD bit = 0), Example 31-4. CRC-SMBus (8-Bit Polynomial with 32-Bit Data, Big-Endian, MOD bit = 1), Example 31-5. CRC-16 (16-Bit Data with 16-Bit Polynomial, Little-Endian, MOD bit = 1), Example 31-6. CRC-32 (32-Bit Polynomial with 32-Bit Data, Little-Endian, MOD bit = 1), and Example 31-7. Data Width Switching (32-Bit Polynomial, Little-Endian, MOD bit = 1).

Equations: Updated Equation 18-5 and Equation 32-3. VSHIFT Calculations.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33AK256MPS306 Family Data Sheet

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