



Product Change Notification: SYST-07GGCO216

Date:

09-Jul-2026

Product Category:

Clock Buffers

Notification Subject:

Data Sheet - ZL40234 - Low Skew, Low Additive Jitter, 4 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output

Affected CPNs:

[SYST-07GGCO216_Affected_CPN_07092026.pdf](#)
[SYST-07GGCO216_Affected_CPN_07092026.csv](#)

Notification Text:

SYST-07GGCO216

Microchip has released a new Datasheet for the ZL40234 - Low Skew, Low Additive Jitter, 4 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output of devices. If you are using one of these devices please read the document located at [ZL40234 - Low Skew, Low Additive Jitter, 4 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output](#).

Notification Status: Final

Description of Change:

Application:

Added PCIe Gen 7 to first bullet point.

Figure 3-13:

Added a new scope image ("491.52 MHz HCSL Phase Noise:") after Figure 3-12, making it the new Figure 3-13. Renumbered the "156.25 MHz LVPECL Phase Noise" scope image from Figure 3-13 to

Figure 3-14 and renumbered all following images within the Typical Device Performance Section accordingly.

Table 4-14:

Updated the HCSL outputs for VDDO = 3.3V output frequency maximum value from 400 MHz to 800 MHz. Added PCIe 6.0 and PCIe 7.0 additive jitter, additive RMS jitter, and noise floor values to the table, too.

Table 4-15:

Updated the HCSL outputs for VDDO = 2.5V output frequency maximum value from 400 MHz to 800 MHz. Added PCIe 6.0 and PCIe 7.0 additive jitter, additive RMS jitter, and noise floor values to the table, too.

Microchip Information:

Updated back matter with most current version.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 09 Jul 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ZL40234 - Low Skew, Low Additive Jitter, 4 Output LVPECL/LVDS/HCSL Fanout Buffer with One LVCMOS Output

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