



## Product Change Notification: SYST-05KRRP991

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**Date:**

08-Sep-2025

**Product Category:**

Digital Signal Controllers

**Notification Subject:**

Data Sheet - dsPIC33AK512MPS512 Family Data Sheet

**Affected CPNs:**

[SYST-05KRRP991\\_Affected\\_CPN\\_09082025.pdf](#)

[SYST-05KRRP991\\_Affected\\_CPN\\_09082025.csv](#)

**Notification Text:**

SYST-05KRRP991

Microchip has released a new Datasheet for the dsPIC33AK512MPS512 Family Data Sheet of devices. If you are using one of these devices please read the document located at [dsPIC33AK512MPS512 Family Data Sheet](#).

**Notification Status:** Final

**Description of Change:**

Revision B

This revision incorporates the following updates:

- Sections:

- Updated High-Performance dsPIC33A DSP CPU, Security Features, Peripheral Features, Functional Safety Support, 3.4. Buck Converter Guidelines and Considerations, 2.6 ICSP Pins, 3.8 External Oscillator Layout Guidance, 3.9 Oscillator Value Conditions on Device

Start-up, 3.11 Targeted Applications, 4.3.10.3. Stack Pointer Overflow, 4.3.11.1 Byte to Word Conversion, 4.3.12.3.3 Data Space Write Saturation, 4.3.16.4. Data Alignment 4.4. Prefetch Branch Unit (PBU), 4.4.3.3. PBU Data Error Handling, 6. Data Memory, 6.4.2. Data Space Address Generation Units (AGUs), 6.4.7 MBIST Overview, 7.3.2.2.2. Word Programming, 7.3.2.2.3. Bus Mastered Row Programming, 7.3.4 NVM CRC, 7.4 Flash Dual Partition, 7.4.1. Architectural Overview, 7.4.2.2.1 Configuring Active/Inactive Partitions, 7.4.3.2. Word Programming (Active Partition), 7.4.3.3. Row Programming (Active Partition), Panel Swap Code Sequence, 9. Security Module, 11.9.1.4. Stack Error Trap, 11.10.4.1. Interrupt Latency, 12.4.4.3 Input Mapping, 13.7.4. I/O Integrity Module Operations in Idle Mode, 13.4.3 Primary Oscillator (POSC), 13.4.7.5.1. Catastrophic Fault Injection, 14. Direct Memory Access (DMA) Controller, 14.4.12. Bit Manipulation, 14.6.1.4. Pattern Match Interrupt, 15.2. Features, 15.6.1. Clock Configuration, 16. High-Resolution PWM with Fine Edge Placement, 16.2.2.2. PWM Operating Modes, 16.4.2.2.4. LLC Resonant Converter Mode, Software PCI Control, 16.4.2.8. Software Override, 16.4.3.2. LFSR – Linear Feedback Shift Register, 16.5.2.4.3. Software Trigger, 17. 40 MSPS Analog-to-Digital Converter (ADC), 17.4.4. Conversions, 17.4.7. Comparator, 17.4.8. Interrupts, 17.4.10. Results Formatting, 17.4.13. Power-Saving Mode, 17.6. Effects of Reset, 18. Integrated Touch Controller (ITC), 18.3.12. CVD Capacitors Array, 19.3.12. CVD Capacitors Array, 19.4.2. Pulse Density Modulation (PDM) DAC, 19.4.3.2. Slope Generator, 19.4.3.2.1. Slope Generation Mode, Hysteretic Mode, 21.4.2.2.1. LIN Commander/Responder Transmit, I2S Audio Host Mode of Operation, PCM/DSP Audio Host Mode of Operation, 22.4.2.6.2. Host Mode Clocking and MCLK, I2S Audio Host Mode of Operation Using REFCLKO, 27. Capture/Compare/PWM/Timer Modules (SCCP/MCCP), 33.2. Architectural Overview, 33.4.3. Power Modes, 33.4.4. Differential Input and 33.4.5. Input Offset Trim.

– Added High-Resolution Mode Data Registers, High-Resolution Period Synchronization, Runt Pulse Indication, Calibration, Gain Error Calibration, Single Trigger Mode, Retriggerable Mode, CRC Control Register, CRC Error Status, Output Override Behavior in Complementary Output Mode with Priority Overrides and Force-On, Output Override Behavior in Complementary Output Mode with PWMxL’s Max On-time Adjustment, Software Trigger, Trigger Count (Burst Mode), Data Buffering, Sleep and Idle Mode, DAC Output Filter Modes and Static Operating Mode.

– Removed Read-After-Write Dependency Rules, Instruction Stall Cycles, Enable Output Monitor, Ping-Pong Transmit Steady State, Ping-Pong Transmit Initialization, Ping-Pong Receive Steady State, Ping-Pong Receive Initialization and Minimum PWM Period and Pulse Width.

- Tables:

– Updated Table 1-1. Pinout I/O Descriptions, Table 4-1. MCU Instruction Addressing Mode Definitions, Table 4-6. Accumulator Overflow and Saturation Status Bits, Table 7-2. Flash Boot Mode Select, Table 11-1. Interrupt Vector Details, Table 13-2. CLKGEN Assignment, Table 13-3. Clock Monitor CNTSEL/WINSEL Input Clock Selections, Table 13-5. Clock Monitor CNTSEL/WINSEL Input Clock Selections, Table 14-2. DMA Channel Trigger Sources, Table 15-1. CAN Summary Table, Table 15-2. CLKSEL Clock Selection bit, Table 15-1. PWM Summary Table, Table 15-2. Auxiliary PWM Summary Table, Table 15-4. PCI Source Selection (PSS), Table 15-5. PWM Peripheral Pin Select Mapping, Table 15-9. Override Behavior in Complementary Output Mode, Table 15-11. PWM Data Register Update Modes, Table 15-14. Combinatorial Logic Instance Mapping, Table 17-6. Channels with Implemented Secondary Accumulators, Table 26-1. Timer Summary Table, Table 27-3. ICS Input Capture Source Select bits, Table 27-11. Synchronization Sources, Table 29-1. PTG Summary Table, Table 41-6. DC Characteristics: Operating

Current (IDD), Table 41-35. I2Cx Bus Data Timing Requirements (Host Mode), Table 41-36. I2Cx Bus Data Timing Requirements (Client Mode), Specifications.

– Added Auxiliary PWM Summary Table.

• Registers:

– Updated 4.2.17. CPU STATUS Register, 4.5.2.2. HPCSEL0 Register, 4.5.2.3. HPCSEL1 Register, 4.6.7. Floating-Point Exception Address Capture Register, 6.3.2. RAM ECC Status Register, 6.4.7.4. MBIST Control Register, 7.2.1 Nonvolatile Memory (NVM) Control Register, 7.2.3 NVM Write Data 0 Register, 8.1.1. FCP Configuration Register, 8.1.6 FPRxST Configuration Register, 8.1.8. FIRT Configuration Register, 9.2.2. IRT Control Register, 11.4.3 Interrupt Control Register 3, 13.3.2 Oscillator Configuration Register, 13.3.8 PLL Divider Register, 14.3.5. DMA Channel x Control Register, 14.3.7. DMA Channel x Interrupt Register, 14.3.9. DMA Channel x Destination Address Register, 14.3.10. DMA Channel x Count Register, 14.3.11. DMA Channel x Clear Register, 14.3.12. DMA Channel x Set Register, 14.3.13. DMA Channel x Invert Register, 14.3.14. DMA Channel x Mask Register, 15.4.24. CAN 1 FIFO x Control Register, 15.4.25. CAN 1 FIFO x Status Register, 15.4.1. CAN FD x Control Register, 15.4.26. CAN FIFO x User Address Register, 16.3.4.1 PWM Clock Control Register, 16.3.4.8. Combinational Trigger Register, 16.3.4.2 Frequency Scale Register, 16.3.4.3 Frequency Scaling Minimum Period Register, 16.3.4.4 Master Phase Register, 16.3.4.5 Master Duty Cycle Register, 16.3.4.6 Master Period Register, 16.3.4.10 PWM Event Output Control Register y, 16.3.4.41. Auxiliary PWM Event Output Control Register y, 16.3.4.42. Auxiliary PWM Generator x Control Register, 16.3.4.46. Auxiliary PWM Generator x Event 1 Register, 16.3.4.59 Auxiliary PWM Generator x Phase Register, 16.3.4.60. Auxiliary PWM Generator x Duty Cycle Register, 16.3.4.62. Auxiliary PWM Generator x Period Register, 16.3.4.63. Auxiliary PWM Generator x Trigger A Register, 16.3.4.64. Auxiliary PWM Generator x Trigger B

Register, 16.3.4.66. Auxiliary PWM Generator x Trigger D Register, 16.3.4.67. Auxiliary PWM Generator x Trigger E Register, 16.3.4.68. Auxiliary PWM Generator x Trigger F Register, 17.3.1. ADC n Control Register, 17.3.7. ADC n Channel 0 Control Register 1, 18.2.1.13. List x Acquisition and Post-Processing Control Register, 19.3.3. DAC Control Register, 22.3.1. SPIx Control Register 1, 27.4.1. CCPx Control Register 1, 27.4.2. CCPx Control Register 2, 27.4.3. CCPx Control Register 3, 32.3.2. AMPx Control Register 2 and 35.2.4. Peripheral Module Disable 3 Register.

- Figures

- Updated Figure 1-1. dsPIC33AK512MPS512 Family Block Diagram, Figure 2-1. dsPIC33AK512MPS512 Family Block Diagram, Figure 3-2. Example Application Circuit, Figure 4-2. dsPIC33A CPU Programmer's Model, Figure 4-3. Nested Interrupt Context Flow, Figure 4-4. Stack Operation for a CALL Instruction, Figure 4-10. Integer and Fractional Representation of 0x40000001, Figure 4-11. Integer and Fractional Representation of 0xC0000002, Figure 4-16. GOTO & CALL Unconditional PFC Instruction Flow, Figure 7-1. dsPIC33A Program Memory Map, Figure 7-2. dsPIC33A Dual Partition Memory Map, Figure 11-3. Exception Stack Frame, Figure 12-5. IOIM Block Diagram, Figure 16-14. Dual Edge Center-Aligned PWM Mode (MODSEL[2:0] = 111), Figure 16-22. PCI Acceptance Modes, Figure 19-1. High-Speed Analog Comparator Module Block Diagram and Figure 20-2. Quadrature Encoder Interface (QEI) Module Block Diagram.

- Examples: – Updated 17.5.1. Single Conversion, Example 17-3. Integration of the Multiple Samples Example, Example 17-3. Integration of the Multiple Samples Example, Example 17-4. Oversampling Example, Example 17-5. Comparator Example, Example 17-6. Multiple Channels Scan Example, Example 17-7. Second Order Low Pass Filter Example, Example 18-4. CVD Scan of All CVDANx Inputs, Example 19-1. Configuration for Digital Filter, Example 19-2. Configuration of DAC Register, Example 19-3. Triangle Wave Mode

Configuration, Example 26-2. Synchronous External Counter Example Code, Example 26-4. 32-bit Asynchronous Counter Mode Code and Example 34-3. WDT Configuration Example.

• Equations:

– Updated Equation 16-1. PWM Period Calculation, Standard Resolution, Equation 16-2. PWM Duty Cycle, Phase, Trigger and Dead-Time Calculations, Standard Resolution, Equation 16-3. Leading-Edge Blanking Period, Equation 19-1 and Equation 23-2. HDLYC Calculation.

Minor grammatical corrections and formatting changes throughout the document.

**Impacts to Data Sheet:** See above details

**Reason for Change:** To improve productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 08 Sep 2025

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[dsPIC33AK512MPS512 Family Data Sheet](#)

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