Product Change Notification: SYST-03CDXH627

Date:

06-Apr-2026

Product Category:

Digital Signal Controllers

Notification Subject:

Data Sheet - dsPIC33CK512MP608 Family Data Sheet

Affected CPNs:

SYST-03CDXH627_Affected_CPN_04062026.pdf
SYST-03CDXH627_Affected_CPN_04062026.csv

Notification Text:

SYST-03CDXH627
Microchip has released a new Datasheet for the dsPIC33CK512MP608 Family Data Sheet of devices. If you are using one of these devices please read the document located at **dsPIC33CK512MP608 Family Data Sheet**. **Notification Status:** Final **Description of Change:** Revision D (April 2026) • Sections: – Updated “10.1.3 Trigger Source”, “10.2.2 DMA Registers”, “12.4 PWM4H/L Output on Peripheral Pin Select”, “13.1 ADC Features Overview”, “18.2 Setting Baud Rate When Operating as a Bus Host”, “18.3 Client Address Masking”, Product Identification System, 22. Capture/Compare/PWM/Timer Modules (SCCP) and Package Details

– Added: 5.5.1 Activating Flash OTP by ICSP Write Inhibit.

• Tables:

– Updated Table 7-2. Interrupt Vector Details, Table 10-1. DMA Channel Trigger Sources, Table 33-5. Operating Voltage Specifications, Table 33-10. DC Characteristics: Watchdog Timer Delta Current (ΔIWDT), Table 33-26. Internal FRC Accuracy, Table 33-33. SPIx Client Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 0) Timing Requirements, Table 33-34. SPIx Client Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 0), Table 33-35. SPIx Client Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 0), Table 33-38. UARTx Module I/O Timing Requirements, Table 33-39. ADC Module Specifications, Table 33-42. DACx Module Specifications, Table 33-45. Operational Amplifier Specifications, Table 34-5. Operating Voltage Specifications, Table 34-6. DC Characteristics: Operating Current (IDD) (Run), Table 34-7. DC Characteristics: Idle Current (IIDLE), Table 34-9. DC Characteristics: Operating Current (IIDLE), Table 34-13. Watchdog Timer Delta Current (ΔIWDT) and Table 34-22. DACx Module Specifications.

• Figures:

– Updated Figure 7-2. dsPIC33CK512MP608 Alternate Interrupt Vector Table, Figure 11-1. CAN FD Module Block Diagram, Figure 13-1. ADC Module Block Diagram and Figure 22-3. Output Compare x Block Diagram.

• Registers:

– Updated 6.1.2 Reset Control Register, 7.7.3. Interrupt Request Flags Register 2, 7.7.8. Interrupt Request Flags Register 7, 7.7.9. Interrupt Request Flags Register 8, 7.7.12. Interrupt Request Flags Register 11, 7.7.14. Interrupt Enable Register 0, 7.7.15. Interrupt Enable Register 1, 7.7.21. Interrupt Enable Register 7, 7.7.22. Interrupt Enable Register 8, 7.7.24. Interrupt Enable Register 10, 7.7.30. Interrupt Priority Register 3, 7.7.57. Interrupt Priority Register 30, 8.2.2.1 Analog Select for PORTx Register, 8.2.2.2

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12.7.21. PWM Generator x PCI Register Low, 12.7.23. PWM Generator x PCI Register

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– Added Error Trap Origination Address Register Low and Error Trap Origination Address Register High, ADC Channel Trigger 5 Selection Register High, ADC Channel Trigger 6 Selection Register Low and ADC Channel Trigger 6 Selection Register High.

Adds minor text edits throughout document.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 06 Apr 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

dsPIC33CK512MP608 Family Data Sheet

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