Product Change Notification: SYST-02ZLIU791

Date:

05-Feb-2026

Product Category:

32-Bit Microcontrollers

Notification Subject:

Data Sheet - SAM E70/S70/V70/V71 Family Data sheet

Affected CPNs:

SYST-02ZLIU791_Affected_CPN_02052026.pdf
SYST-02ZLIU791_Affected_CPN_02052026.csv

Notification Text:

SYST-02ZLIU791

Microchip has released a new Datasheet for the SAM E70/S70/V70/V71 Family Data sheet of devices. If you are using one of these devices please read the document located at **SAM E70/S70/V70/V71 Family Data sheet**.

Notification Status: Final

Description of Change:

Table 62-1. Rev. J - 02/2026

Section Name or Type Update Description
Features • Updated the QSPI Specifications from 256 to 512 MB of Flash

Configuration Summary • Updated the USART/UART and USART/SPI specifications in Table 1-1, 1-2, 1-3, and 1-4

Power Considerations • Removed an erroneous ground from the table in Power Supplies

Interconnect • Added new notes for the AHBP and AHBS

ARM Cortex-M7 • Updated Table 15-1 in Arm Cortex-M7 Configuration

EEFC • Updated the text in Get Flash Descriptor Command to reflect lock region size

SUPC
• Removed erroneous Register reference in Register Write Protection

• Updated the Register Reset Property for SUPC_MR

• Updated the Register Property for SUPC_WUIR

RSTC
• Added notes to the following sections reflecting a correct watchdog reset:

– General Reset

– RSTC_MR

PMC
• Added a notes to the following sections:

– Core and Bus Independent Clocks for Peripherals

– Startup from Embedded Flash

– Main Crystal Oscillator Failure Detection

• Added a note to the PMC_FSMR Register for improvements to power consumption

• Updated the table for the CSS bitfield in the PMC_PCKx Register

• Updated the table for the GCLKCSS bitfield in the PMC_PCR Register

• Updated the PMC_SLPWLK_ER1 Register with an extended bitfield for PIDx

PIO • Updated the PIO_PCISR Register with the removal of obsolete bitfields

SMC • Added a note to the SMC_WPSR Register regarding Write Protection violations

XDMAC
• Updated the bitfields in the following registers to properly display 24 bits:

– XDMAC_GIE

– XDMAC_GID

– XDMAC_GIM

– XDMAC_GIS

– XDMAC_GE

– XDMAC_GD

– XDMAC_GS

– XDMAC_GRS

– XDMAC_GWS

– XDMAC_GRWS

– XDMAC_GRWR

– XDMAC_GSWR

– XDMAC_GSWS

– XDMAC_GSWF

• Updated the following Registers to properly display offsets:

– XDMAC_CIE

– XDMAC_CID

– XDMAC_CIM

– XDMAC_CIS

– XDMAC_CSA

– XDMAC_CDA

– XDMAC_CNDA

– XDMAC_CNDC

– XDMAC_CUBC

– XDMAC_CBC

– XDMAC_CC

– XDMAC_CDS_MSP

– XDMAC_CSUS

– XDMAC_CDUS

GMAC
• Added the TXLPIEN bitfield to the GMAC_NCR Register

• Removed the GBE bitfield from the GMAC_NCFGR Register

• Added the RXLPIS bitfield to the GMAC_NSR Register

• Updated bitfield naming in the GMAC_UR Register

• Removed obsolete bitfields form the GMAC_TSR Register

• Updated the offsets for the following registers:

– GMAC_ISRPQx

– GMAC_TBQBAPQx

– GMAC_RBQBAPQx

– GMAC_RBSRPQx

– GMAC_ST1RPQx

– GMAC_ST2RPQx

– GMAC_IERPQx

– GMAC_IDRPQx

– GMAC_IMRPQx

– GMAC_ST2CW0x

– GMAC_ST2CW1x

USBHS • Updated the notes in the Description to reflect DMA features and Mixed speed devices

• Updated the USBHS_DEVCTRL Register with a new note for the DETACH bit for High Speed Mode

• Renumbered the DMA_ bitfield in the following registers:

– USBHS_DEVISR

– USBHS_DEVIFR

– USBHS_DEVIMR

– USBHS_DEVIDR

– USBHS_DEVIER

– USBHS_HSTISR

– USBHS_HSTIFR

– USBHS_HSTIMR

– USBHS_HSTIDR

– USBHS_HSTIER

SPI
• Removed an obsolete bitfield from the SPI_SR Register

• Removed obsolete bitfields from the SPI_WPMR Register

QSPI
• Updated Transfer Delays with a new bulleted point about delays

• Removed the TAMPCLR bitfield from the QSPI_MR Register

• Removed obsolete bitfields from the QSPI_IFR Register

TWIHS • Added a note to Repeated Start

SSC • Added a note to Transmit Operations to deal with Unexpected delays

I2SC • Added a new note to I2S Reception and Transmission Sequence

USART
• Added a new note to Baud Rate Generator for performing baud rate detection

• Added a new note to Hardware Handshaking regarding CTS and RTS signals

• Added a note to Bit Error for resetting and re-enabling the transmitter

AFEC
• Removed an erroneous register reference from Register Write Protection

• Updated the Register property for AFEC_CSELR

• Updated the note in the AOFF bitfield of the AFEC_COCR

Register to provide offset error compensation instructions

TRNG
• Updated the following sections to reflect updated NIST Standards:

– Description

– Embedded Characteristics

• Renamed the WAKEY Bitfield to KEY for the TRNG_CR Register

AES • Added the LOADSEED bitfield to the AES_CR Register

Electrical Characteristics for SAM V70/V71 • Updated the following sections with new voltage specifications:

• QSPI Timings

• SMC Timings

• USART SPI Timings

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity.

Change Implementation Status: Complete

Date Document Changes Effective: 05 Feb 2026

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

SAM E70/S70/V70/V71 Family Data sheet

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