CUSTOMER ADVISORY

ADV2515

Agilex™ 3 FPGA and SoC FPGA Known Issue List Document Updates

Issued: 11/26/2025

Description:

Altera is notifying customers of updates to the **Known Issue List** for Agilex 3 devices. Please see the tables below for an overview of some key updates.

The full list of updates is on the revision history at the end of the Known Issue List document which can be downloaded from this link:

https://www.intel.com/content/www/us/en/docs/programmable/855394/current/about-this-document.html

Table 1

Updates Overview: Transceiver	Section
Some reference clock frequencies listed in the drop-down list in the GTS System PLL Clocks IP are not valid for certain output frequencies. Selecting an invalid reference clock option will result in incorrect GTS System PLL Clocks IP output frequencies. The invalid reference clock frequency options are available in Quartus® Prime Pro Edition software version 25.3 and earlier. The invalid options will be removed in the future release of the Quartus® Prime Pro Edition software version.	2.1.1.5

Table 2

Updates Overview: Hard Processor System (HPS)	Section
The GICv3 ITS cannot initialize MSI-X interrupts because the configuration of the GIC ACE slave and master ports uses a 32-bit address width, which does not match the subsystem's physical address width. This affects system with DDR memory larger than 2 GB or physical address range above 4 GB.	2.1.3.4
SD/eMMC Host Controller Capabilities Register provides incorrect information regarding 8-bit Embedded Device Support	2.1.3.5

Recommended Actions:

Customers are requested to review the change and determine the impact on their designs.

For questions or support, please contact your local Sales/FAE representative, or submit a support ticket at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

Agilex 3 FPGA and SoC FPGA Devices

The list of affected ordering part numbers (OPNs) can be downloaded in Excel form: https://cdrdv2.intel.com/v1/dl/getContent/869630

Contact:

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Customer Notifications Subscription:

If you would like to receive customer notifications by email, please follow the instructions in ADV 2209

Altera references J-STD-046 guidelines for PCN.

In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from date of notification.

Revision History:

Date	Rev	Description
11/26/2025	1.0	Initial Release