Product Change Notification

Product Change Notification Number: WC131402A (REVISED 07/26/13) **Notification Date:** April 24, 2013

Removed ATxmega64D3-MHR from the Table Below

Title: Die Revision Change for ATxmega64D3

Product Identification:

ATxmega64D3-AU

ATxmega64D3-AUR

Reason for Change:			
☒ Material / Composition	☒ Design / Firmware	☐ Manufacturing Location
☐ Processing / Manufacturing	☐ Logistics	☒ Quality / Reliability

Change Description:

This notification is to advice our customers that Atmel will introduce new revisions of the AVR microcontroller products listed above. The new revisions are package and pin compatible to the existing revisions. They are introduced in order to remove errata and enhance the product. Actual devices changes are minimal, but for your reference they are listed here together with enhancements that are a pure superset of existing functions.

Samples are available as listed below and can be ordered through Atmel Sample Center by logging on to https://samples.atmel.com/scripts/samplecenter.dll?atmel?cmd=menu

Specific ordering codes for new die revision samples only are shown in the table below, and are available for sample orders only until the proposed first shipment date. For all production orders, only standard existing ordering codes will be accepted.

Part number	Ordering code for samples
ATxmega64D3-AU (Note: **No** Tape&Reel samples available for AU package)	ATxmega64D3-AUK
~~ATxmega64D3-MHR~~ ~~(Note: Only Tape&Reel samples available for MH package)~~	~~ATxmega64D3-MHRK~~

Note that the **K** in sample ordering codes will not be marked on the package.

Changes

The new revision change the following:

- Reduced current consumption
- Increased maximum ADC sample rate
- Reduced Analog Comparator propagation delay
- Brown-Out Detection (BOD) levels.
- The BOD is forced on only during selected NVM programming commands
- Chip erase time during programming
- 32kHz internal ULP oscillator frequency
- Access to unused registers removed
- Bonding wire material has changed from gold to copper

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

New configuration options and functions

The new revision includes new configuration options and functions that are a superset of existing functions. This means that existing software for the existing device revisions will work on the new revision without changing existing configuration or enabling new functions.

See Appendix 1 for more details on changes.

See Appendix 2 for more details on added functions.

Identification Method to Distinguish Change:

For packages where space allows for die ID to be part of marking, new revision material is identified as 359P9I.

Qualification Data:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable
Samples:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable

Quantifiable Impact on Quality & Reliability:

None

Proposed First Ship Date*: July 19, 2013

**The Proposed First Ship Date is the forecasted date that a customer may expect to receive changed product. This is determined by the estimated date of inventory depletion on the PCN issue date. This may be affected by fluctuations in supply and demand. Consequently, although customers should be prepared to receive changed product on this date, Atmel will continue to ship pre-changed product until a time in which inventory has been depleted. This may result in pre-changed product being shipped to customers after this forecasted date.*

Atmel Contact: Please contact your Atmel Sales Representative or Distributor for additional information (when replying via e-mail please include PCN number in subject line).

CUSTOMER ACKNOWLEDGEMENT OF RECEIPT: Atmel requests you acknowledge receipt of this PCN. Please complete and email to pcnadm@atmel.com and the Atmel Contact listed above. In your acknowledgement, you can grant approval or request additional information. **Atmel will deem this change accepted unless specific conditions of acceptance are provided in writing within 30 days from the date of this notice.**

Company:	
Name:	
Title:	
Date:	
Email Address:	
Location:	
Comments:	

Appendix 1: Change Description Details

Reduced current consumption in Active and Idle mode

The table below lists the typical and maximum current consumption in the existing and new revision.

Parameter	Condition		Existing revisions			New revision			Units
			Min	Typ	Max	Min	Typ	Max	
Active power consumption	32kHz, Ext. Clk	V_{CC} = 1.8V		25			50		µA
		V_{CC} = 3.0V		71			130		
	1MHz, Ext. Clk	V_{CC} = 1.8V		317			215		
		V_{CC} = 3.0V		697			475		
	2MHz, Ext. Clk	V_{CC} = 1.8V		613	800		445	600	
		V_{CC} = 3.0V		1.3	1.8		0.95	1.5	mA
	32MHz, Ext. Clk			15.7	18		7.8	12	
Idle power consumption	32kHz, Ext. Clk	V_{CC} = 1.8V		4.0			2.8		µA
		V_{CC} = 3.0V		7.0			3.0		
	1MHz, Ext. Clk	V_{CC} = 1.8V		112			46		
		V_{CC} = 3.0V		215			92		
	2MHz, Ext. Clk	V_{CC} = 1.8V		224	350		93	225	
		V_{CC} = 3.0V		430	600		184	350	
	32MHz, Ext. Clk			6.9	8.0		2.9	5.0	
Power-down power consumption	T = 25°C			0.1	3.0		0.07	1.0	
	T = 85°C			1.8	5.0		1.3	5.0	
	WDT and sampled BOD enabled, T = 25°C			1.3	6.0		1.4	2.0	
	WDT and sampled BOD enabled, T = 85°C			2.7	10.0		2.6	6.0	
Power-save power consumption	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2			1.7		
		V_{CC} = 3.0V		1.3			1.8		
	RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	4.0		0.7	2.0	
		V_{CC} = 3.0V		0.7	4.0		0.8	2.0	
	RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		na	na		0.9	3.0	
		V_{CC} = 3.0V		1.2	na		1.1	3.0	
Reset power consumption	Current through RESET pin substracted	V_{CC} = 3.0V		1300			120		

Increased ADC maximum samples rate

The maximum ADC clock frequency and sample rate is increased, as shown in the table below.

Parameter	Existing revisions			New revision			Units
	Min	Typ	Max	Min	Typ	Max	
ADC clock frequency	na		1400	100		1800	kHz
ADC samples rate	na		200	16		300	kSPS

Reduced Analog Comparator propagation delay

The Analog Comparator propagation delay is reduced, as shown in the table below.

Parameter	Condition	Existing revisions			Units
		Min	Typ	Max	
Propagation delay	V_{CC} = 3.0V, T=85°C		na	na	ns
Propagation delay	V_{CC} = 1.6V-3.6V, T=25°C		175		ns

Parameter	Condition	New revision			Units
		Min	Typ	Max	
Propagation delay	V_{CC} = 3.0V, T=85°C		20	40	ns
Propagation delay	V_{CC} = 3.0V, T=25°C		17		ns

Brown-Out Detection (BOD) levels.

The table below lists the BOD levels in the existing revisions, and the expected BOD levels in the new revision.

Parameter	Existing revisions			New revision			
	Min	Typ	Max	Min	Typ	Max	Units
BOD level 0 falling Vcc	1.62	1.63	1.7	1.50	1.60	1.70	V
BOD level 1 falling Vcc		1.9			1.8		
BOD level 2 falling Vcc		2.17			2.0		
BOD level 3 falling Vcc		2.43			2.2		
BOD level 4 falling Vcc		2.68			2.4		
BOD level 5 falling Vcc		2.96			2.6		
BOD level 6 falling Vcc		3.22			2.8		
BOD level 7 falling Vcc		3.49			3.0		

The BOD forced on only during selected NVM programming commands

For existing revisions the BOD is forced on for all Non-Volatile Memory (NVM) programming. For the new revision, the BOD is only forced on during chip erase and when the PDI is enabled. For other NVM programming operations, the POR threshold voltage (V_{POT+}) is the limit for aborting.

Chip erase time during programming

For the existing revisions the chip erase time is about 40ms, while in the new revision this is increased to 55ms.

32kHz internal ULP oscillator frequency

The frequency of the 32kHz internal ULP oscillator is increased to match its nominal frequency with guarnted accuracy.

Parameter	Condition	Existing revisions			New revision			Units
		Min	Typ	Max	Min	Typ	Max	
Factory calibrated frequency			26			32		kHz
Factory calibration accuracy	V_{CC} = 3.0V, T= 85°C	na		na	-12		12	%
Accuracy		na		na	-30		30	

Removed registers

The below register bits have been removed as they are unused.

Register Name	Register Bit	Function
COMP0	COMP[7:0]	Oscillator Compare Register 0

Appendix 2: Added Functions

Clock System

- Alternate pin location for TOSC1 and TOSC2 pins for 32.768 kHz crystal connection on devices with shared TOSC and XTAL location today.
- A divide by two option for the PLL output.
- PLL lock failure detection with optional non maskable interrupt for improved safety and robustness.
- Non-prescaled Real Time Counter clock source options: External clock from TOSC1, 32.768 kHz from TOSC, and the 32.768 kHz from the 32.768 kHz Internal Oscillator.
- Higher drive option for external crystal oscillator to support higher load crystals.
- The 32 MHz internal oscillator can be tuned to run at any frequency between 30 MHz and 55 MHz.

I/O Ports

- Alternate pin locations for Timer/Counter 0 Compare Channels, USART0 and SPI.
- Alternate pin locations for the Peripheral Clock and Event output functions.
- The Real Time Counter clock can be output to a port pin.
- Any Event Channel can be output to a port pin.

Two Wire Interface

- The SDA Hold time can be increased and configured in order to be SMBUS compliant.

Analog to Digital Converter

- Automatic input channel scan.
- VCC/2 voltage reference option.
- 1/2x (divide by two) gain stage setting.
- Internal Ground can be used as negative input in differential mode with and without gain.
- Sample time is configurable

Analog Comparator

- Analog Comparator 1 can be output on a port pin.
- Added constant current source.

CRC16/CRC32 Generator

- A CRC16/CRC32 Module that supports CRC16 (RC-CCITT) and CRC-32 (IEEE 802.3).

16-bit Timer / Counter 0

- Split mode that enable a system of two 8-bit Timer/Counters with 4 PWM channels each.

AWeX

- Hi-Res+ option to allow PWM resolution to be increased with 8x (3-bit)

Power Management

- Possibility to enable sequential start of the internal modules used for ADC and Analog Comparator in order to reduce the peak start-up current.