



Product/Process Change Notice - PCN 22_0212 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: LTC4270 Datasheet Limit Change

Publication Date: 29-Aug-2022

Effectivity Date: 01-Dec-2022 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change:

Please be advised that Analog Devices has made a minor change to the LTC4270 product datasheet to facilitate improvement in manufacturing capability. The changes are shown on the attached pages of the marked-up datasheet.

Electrical Characteristics table changes (page 4 of datasheet):

1. GATE Pin Pull-Down Current Port off, VGATEn = VEE + 5v, minimum spec limit changed from 0.4mA to 0.3mA. Also, temperature condition changed from Tri-temperature to Room temperature only.
2. GATE Pin Pull-Down Current Port off, VGATEn = VEE + 1v, minimum spec limit changed from 0.08mA to 0.06mA. Also, temperature condition changed from Tri-temperature to Room temperature only.

Reason For Change:

To facilitate improvement in manufacturing capability.

Impact of the change (positive or negative) on fit, form, function & reliability:

This datasheet change does not impact the fit, form, function, or reliability of the LTC4270

Product Identification *(this section will describe how to identify the changed material)*

Product shipped after effectivity date will be tested to the new limits.

Can be identified with date code and lot traceability identification.

Summary of Supporting Information:

Changes will be reflected on the new product datasheet. See changes on Electrical Characteristics table on page 4.

Supporting Documents

Attachment 1: Type: Datasheet Specification Comparison

ADI_PCN_22_0212_Rev_-LTC4270 Datasheet Marked-up Page.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:
PCN_Americas@analog.com

Europe:
PCN_Europe@analog.com

Japan:
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Rest of Asia:
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Appendix A - Affected ADI Models**Added Parts On This Revision - Product Family / Model Number (10)**

LTC4270 / LTC4270AIUKG#PBF	LTC4270 / LTC4270AIUKG#TRPBF	LTC4270 / LTC4270BIUKG#PBF	LTC4270 / LTC4270BIUKG#TRMPBF	LTC4270 / LTC4270BIUKG#TRPBF
LTC4270 / LTC4270CIUKG#PBF	LTC4270 / LTC4270CIUKG#TRPBF	LTC4271_70 / LTC4271IUF#PBF	LTC4271_70 / LTC4271IUF#TRMPBF	LTC4271_70 / LTC4271IUF#TRPBF

Appendix B - Revision History

Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	29-Aug-2022	01-Dec-2022	Initial Release

Analog Devices, Inc.

DocId:9004 Parent DocId:None Layout Rev:8

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $\text{AGND} - V_{EE} = 54\text{V}$ and $V_{DD} - \text{DGND} = 3.3\text{V}$ unless otherwise noted. (Notes 3 & 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{EE}	Main PoE Supply Voltage	AGND – V_{EE} For IEEE Type 1 Compliant Output For IEEE Type 2 Compliant Output For LTPoE++ Compliant Output	● ● ●	45 51 54.75	57 57 57	V
	Undervoltage Lock-Out	V_{EE}	●	20	25	V
	V_{DD}	$V_{DD} - \text{DGND}$	●	3.0	3.3	V
	Undervoltage Lock-Out	$V_{DD} - \text{DGND}$			2.7	V
V_{CAP1}	Internal Regulator Supply Voltage	$V_{CAP1} - \text{DGND}$			1.84	V
V_{CAP2}	Internal Regulator Supply Voltage	$V_{CAP2} - V_{EE}$			4.3	V
I_{EE}	V_{EE} Supply Current	$(\text{AGND} - V_{EE}) = 55\text{V}$	●	9	15	mA
R_{EE}	V_{EE} Supply Resistance	$V_{EE} < 15\text{V}$	●		12	k Ω
I_{DD}	V_{DD} Supply Current	$(V_{DD} - \text{DGND}) = 3.3\text{V}$	●		10	mA

Detection

	Detection Current – Forced Current	First Point, $\text{AGND} - V_{OUTn} = 9\text{V}$ Second Point, $\text{AGND} - V_{OUTn} = 3.5\text{V}$	● ●	220 143	240 160	260 180	μA μA
	Detection Voltage – Forced Voltage	$\text{AGND} - V_{OUTn}$, $5\mu\text{A} \leq I_{OUTn} \leq 500\mu\text{A}$ First Point Second Point	● ●	7 3	8 4	9 5	V V
	Detection Current Compliance	$\text{AGND} - V_{OUTn} = 0\text{V}$	●		0.8	0.9	mA
V_{OC}	Detection Voltage Compliance	$\text{AGND} - V_{OUTn}$, Open Port	●		10.4	12	V
	Detection Voltage Slew Rate	$\text{AGND} - V_{OUTn}$, $C_{PORT} = 0.15\mu\text{F}$	●			0.01	V/μs
	Min. Valid Signature Resistance		●	15.5	17	18.5	k Ω
	Max. Valid Signature Resistance		●	27.5	29.7	32	k Ω

Classification

V_{CLASS}	Classification Voltage	$\text{AGND} - V_{OUTn}$, $0\text{mA} \leq I_{OUTn} \leq 50\text{mA}$	●	16.0	20.5	V	
	Classification Current Compliance	$V_{OUTn} = \text{AGND}$	●	53	61	67	mA
	Classification Threshold Current	Class 0-1 Class 1-2 Class 2-3 Class 3-4 Class 4-Overcurrent	● ● ● ● ●	5.5 13.5 21.5 31.5 45.2	6.5 14.5 23 33 48	7.5 15.5 24.5 34.9 50.8	mA
V_{MARK}	Classification Mark State Voltage	$\text{AGND} - V_{OUTn}$, $0.1\text{mA} \leq I_{CLASS} \leq 5\text{mA}$	●	7.5	9	10	V
	Mark State Current Compliance	$V_{OUTn} = \text{AGND}$	●	53	61	67	mA

Gate Driver

	GATE Pin Pull-Down Current	Port Off, $V_{GATEn} = V_{EE} + 5\text{V}$ Port Off, $V_{GATEn} = V_{EE} + 1\text{V}$	✗ ✗	0.4 0.08	0.3 0.12		mA
	GATE Pin Fast Pull-Down Current	$V_{GATEn} = V_{EE} + 5\text{V}$			30		mA
	GATE Pin On Voltage	$V_{GATEn} - V_{EE}$, $I_{GATEn} = 1\mu\text{A}$	●	8	12	14	V