# Product/Process Change Notice - PCN 23_0136 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

| | |
|---|---|
| **PCN Title:** | LTC7878 Data Sheet Change |
| **Publication Date:** | 15-Aug-2023 |
| **Effectivity Date:** | 17-Nov-2023 *(the earliest date that a customer could expect to receive changed material)* |
| **Revision Description:** | Initial Release. |

## Description Of Change:

Minor changes to the LTC7878 product datasheet as shown on the attached pages of the marked-up datasheet.
1. Electrical Characteristics table changes (page 3 of datasheet):
DRVcc Under Voltage Lockout: Change upper limit from 4.5V to 4.62V.
2. Block Diagram (page 10 of the datasheet):
Change (gmb - gmb) to (gm-gmb)
3. Change Iload formula on page 15
4. Application Information (page 19 of datasheet):
Change DBST1 to DBST2

## Reason For Change:

To facilitate improvement in manufacturing capability and correct typographical errors.

## Impact of the change (positive or negative) on fit, form, function & reliability:

This data sheet change does not impact the fit, form, function, or reliability of the device.

## Product Identification *(this section will describe how to identify the changed material)*

Product shipped after effectivity date will be tested to the new limits.
They can be identified with date code and lot traceability identification.

## Summary of Supporting Information:

Qualification is not required. Changes will be reflected on the new product data sheet revision A.

## Supporting Documents

**Attachment 1: Type**: Datasheet Specification Comparison

ADI_PCN_23_0136_Rev_-_LTC7878_Datasheet Marked-up.pdf...

Note: If applicable, the device material declaration will be updated due to material change.

## ADI Contact Information:

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

| **Americas:** | **Europe:** | **Japan:** | **Rest of Asia:** |
|---|---|---|---|

| | | | |
|---|---|---|---|
| PCN_Americas@analog.com | PCN_Europe@analog.com | PCN_Japan@analog.com | PCN_ROA@analog.com |

## Appendix A - Affected ADI Models:

### Added Parts On This Revision - Product Family / Model Number (2)

LTC7878 / LTC7878AUH#PBF

LTC7878 / LTC7878AUH#TRPBF

## Appendix B - Revision History:

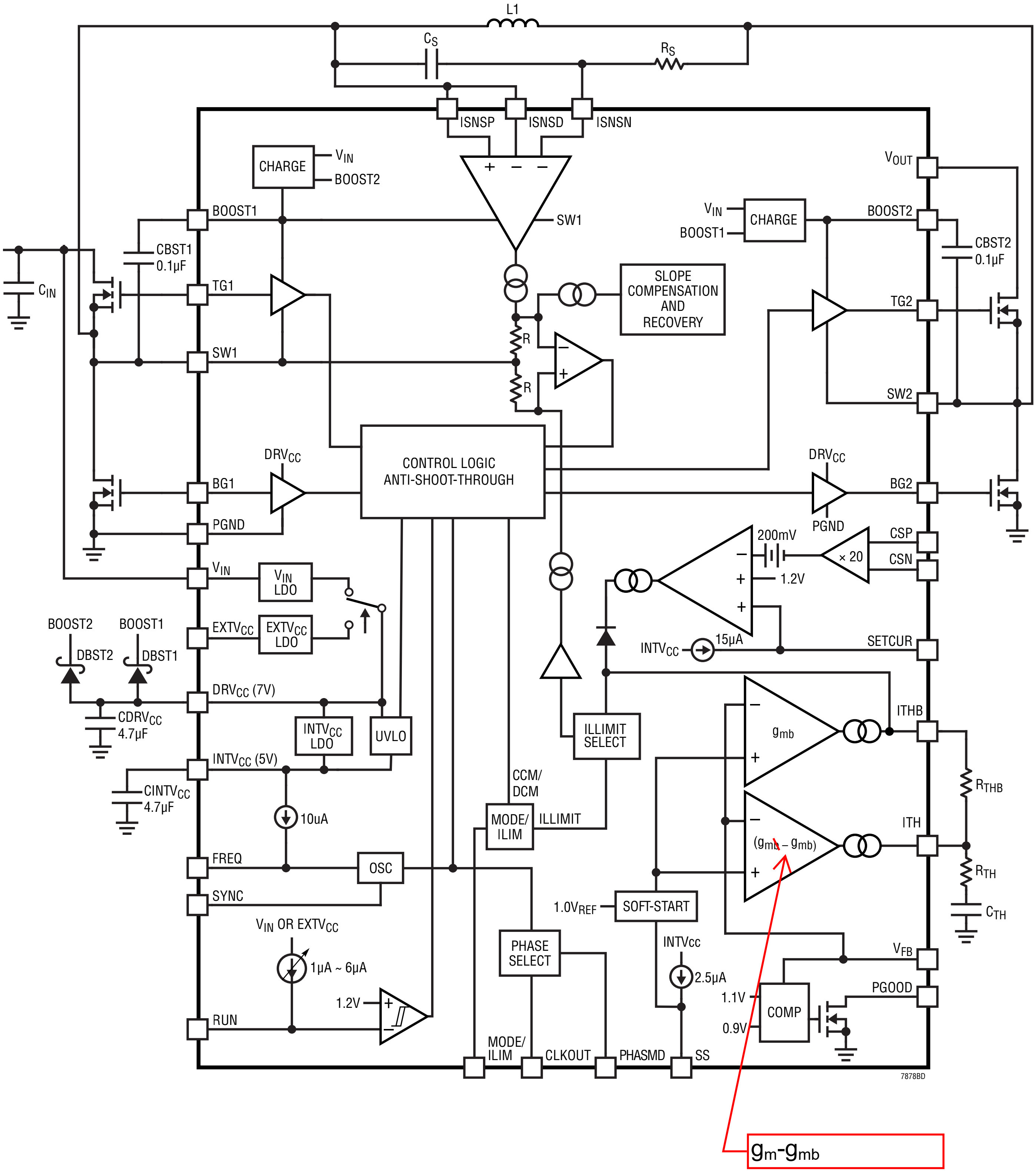
| Rev | Publish Date | Effectivity Date | Rev Description |
|---|---|---|---|
| Rev. - | 15-Aug-2023 | 17-Nov-2023 | Initial Release. |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$. , $V_{IN} = 12V$, RUN > 1.25V unless otherwise noted. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Bias Supply ($V_{IN}$, $EXTV_{CC}$)** | | | | | | | |
| $V_{IN}$ | Bias Input Supply Operating Voltage Range | | | 5 | | 70 | V |
| EXTVcc | Auxiliary Bias Voltage Operating Range | | | 5 | | 70 | V |
| $I_Q$ | $V_{IN}$ Supply Current (Shutdown Mode) | $V_{IN}$ = 5V, RUN = 0V, $EXTV_{CC}$ = 0V | | | 70 | 100 | µA |
| | $V_{IN}$ Supply Current (Standby Mode) | $V_{IN}$ = 5V, RUN = 0.9V, $EXTV_{CC}$ = 0V | | | 3 | | mA |
| **Controller Operation** | | | | | | | |
| $V_{OUT}$ | Output Voltage Operating Range | | | 1 | | 70 | V |
| $V_{FB}$ | Regulated Feedback Voltage | (Note 4) ITH, ITHB Voltage = 1.2V | ● | 0.99 | 1.00 | 1.01 | V |
| $IV_{FB}$ | $V_{FB}$ Pin Current | (Note 4) | | | –50 | –100 | nA |
| $V_{REFLNREG}$ | Reference Voltage Line Regulation | (Note 4), $V_{IN}$ = 12V to 72V | | | 0.01 | 0.2 | % |
| $V_{LOADREG}$ | Output Voltage Load Regulation | Measure in Servo Loop, ITH = ITHB, $\Delta I_{TH}$ Voltage = 1.2V to 1.8V | | | 0.05 | 0.2 | % |
| | | Measure in Servo Loop, ITH = ITHB, $\Delta I_{TH}$ Voltage = 1.2V to 0.6V | | | –0.05 | –0.2 | % |
| $g_m$ | Error Amplifier Transconductance $g_m$ | (Note 4) ITH = ITHB = 1.2V, Sink/Source = 10µA | | | 2 | | mmho |
| $g_{mb}$ (Buck) | Error Amplifier Transconductance $g_{mb}$ | (Note 4) ITH = ITHB = 1.2V, Sink/Source = 10µA | | | 1 | | mmho |
| $UVLO\_DRV_{CC}$ | $DRV_{CC}$ Undervoltage Lockout | $DRV_{CC}$ Ramping Down | | 3.9 | 4.3 | ~~4.5~~ 4.62 | V |
| UVLO_DRV_HYS | $DRV_{CC}$ Undervoltage Hysteresis | | | | 0.35 | | V |
| $UVLO\_INTV_{CC}$ | $INTV_{CC}$ Undervoltage Lockout | $INTV_{CC}$ Ramping Down | | | 3.95 | | V |
| UVLO_INTV_HYS | $INTV_{CC}$ Undervoltage Hysteresis | | | | 0.45 | | V |
| $V_{RUN}$ | RUN Pin Threshold 1 (Shutdown to Standby)<br>RUN Pin Threshold 2 (Standby to On) | $V_{RUN}$ Rising<br>$V_{RUN}$ Rising | | 0.3<br>1.1 | 0.57<br>1.2 | <br>1.3 | V<br>V |
| $I_{RUN}$ | RUN Pin Source Current | $V_{RUN}$ <0.57V<br>0.57V < $V_{RUN}$ < 1.2V<br>$V_{RUN}$ > 1.2V | | | 1<br>2<br>6 | | µA<br>µA<br>µA |
| $I_{SS}$ | Soft-Start (SS Pin) Source Current | | | | 2.5 | | µA |
| DMAX_BG2 | Maximum Duty Cycle of Boost Mode (BG2) | | | | 90 | | % |
| **Inductor Current Sensing** | | | | | | | |
| $V_{SENSE(ILMAX)}$ | Maximum Inductor Peak Current Sense Threshold | MODE/ILIM < $INTV_{CC}$/2, ITH = ITHB = 2.1V, $V_{ISNSP}$– $V_{ISNSD}$ = 25mV | ● | 18 | 25 | 32 | mV |
| | | MODE/ILIM > $INTV_{CC}$/2, ITH = ITHB = 2.1V, $V_{ISNSP}$ – $V_{ISNSD}$ = 50mV | ● | 40 | 50 | 60 | mV |
| | | MODE/ILIM < $INTV_{CC}$/2, ITH = ITHB = 2.1V, $V_{ISNSP}$ = $V_{ISNSD}$ | ● | 92 | 100 | 108 | mV |
| | | MODE/ILIM > $INTV_{CC}$/2, ITH = ITHB = 2.1V, $V_{ISNSP}$ = $V_{ISNSD}$ | ● | 190 | 200 | 210 | mV |
| $I_{ISNSD}$ | ISNSD Pin Leakage Current | | | | 0 | ±0.1 | µA |
| $I_{ISNSN}$ | ISNSN Pin Leakage Current | | | | 0 | ±0.1 | µA |
| **Input/Output Average Current Regulation** | | | | | | | |
| $I_{CSP}$ | CSP Pin Input Current | $V_{CSP}$ = $V_{CSN}$ > 5V, $V_{CSP}$ – $V_{CSN}$ = 50mV | | | 14 | 20 | µA |
| $I_{CSN}$ | CSN Pin Input Current | $V_{CSP}$ = $V_{CSN}$ > 5V, $V_{CSP}$ – $V_{CSN}$ = 50mV | | | 14 | 20 | µA |
| $\Delta I_{CS}$ | CSP/CSN Pin Current Mismatch | $V_{CSP}$ = 12V, $V_{CSP}$ – $V_{CSN}$ = 50mV | | | 0.05 | ±1 | µA |
| $V_{MAX(IAVG)}$ | Maximum Average Current Limit | $V_{CSP}$ = 12V | ● | 46.5 | 50 | 53 | mV |
| $I_{SETCUR}$ | SETCUR Pin Output Current | | | 14 | 15 | 16 | µA |

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7878 application circuit. Detailed external components may be referred to the Figure 8. External component selection is driven by the load requirement and begins with the selection of the inductor value and DCR. Next, the power MOSFETs are selected. Finally, $C_{IN}$ and $C_{OUT}$ are selected. This circuit can be configured for operation up to an input voltage of 70V.

### Inductor Selection and DCR Current Sensing

The inductor selection and operating frequency are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values but with higher switching losses. The inductor value also has a direct effect on ripple current. Since LTC7878 is a constant-frequency peak current mode controller, the inductor peak current is regulated and limited cycle-by-cycle. The inductor should be selected with saturation current higher than the maximum peak current. The maximum output DC current in the buck mode is the peak inductor current minus half of the ripple current. In the boost mode, the maximum output DC current varies with duty cycle and ripple current. Too large ripple current will reduce the maximum output current and too small ripple may cause the small current sense signal and more sensitive to the switching noise. Typically, set the inductor current ripple $\Delta I_L$ to 30% to 60% of the maximum DC inductor current at the nominal input voltage is a good starting point. If the buck-boost converter only operates in buck mode and buck-boost mode, the maximum DC inductor current is about the maximum output load current. Otherwise, the maximum DC inductor current is the inductor current in the boost mode with minimum $V_{IN}$ at the maximum load condition. And it can be calculated as:

$$I_L = I_{LOAD(MAX)} \frac{V_{OUT}}{\xcancel{V_{OUT} -} V_{IN}}$$

LTC7878 uses the inductor DCR (DC Resistance) for current sensing and close loop regulation. After selecting the inductance and saturation current, the DCR of the inductor also need to be properly chosen to achieve the required output current and current limit. To sense the inductor current with a large DCR, ISNSD pin may be short to the ISNSP pin to achieve 100mV or 200mV current sense threshold limits. Choose the DCR of the inductor so that the peak current is less than the saturation current but higher than the maximum DC current plus the ripple current.

$$DCR \le \frac{V_{SENSE(MAX)}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

Filter components, especially capacitors, must be placed close to the LTC7878, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 3). And in Figure 4, the external R1 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR. C1 is usually selected to be in the range of 0.047µF to 0.47µF. For example, a 4.7µH/10mΩ inductor and C1= 0.047uF, the R1 should be L/(DCR • C1) = 10kΩ. The maximum peak inductor current is $V_{SENSE}$/DCR = (100mV or 200mV)/10mΩ = 10A or 20A depend on the MODE/ILIM pin setup. To further tune the current limit, another resistor may be paralleled with C1 to form a resistor divider with R1 and scale the sensed voltage. Refer to the standard DCR setup in buck controller data sheet (e.g. LTC3855) for details.

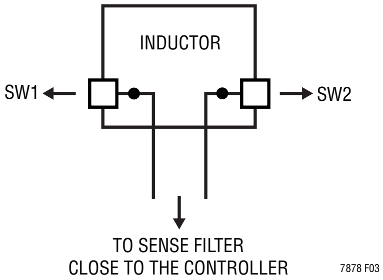


**Figure 3. Sense Lines Placement with Inductor DCR**

## APPLICATIONS INFORMATION

by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = {\frac{I_{OUT(MAX)} \cdot V_{OUT}}{V_{IN}}}^{2} \cdot \rho\tau \cdot R_{DS(ON)} \cdot \frac{V_{IN}}{V_{OUT}}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \cdot R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

### Top MOSFET Driver Supply

Refer to the Block Diagram, the external bootstrap capacitors $C_{BST1}$ and $C_{BST2}$ connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside MOSFET. When the top switch A turns on, the switch node SW1 rises to $V_{IN}$ and the BOOST1 pin rises to approximately $V_{IN} + DRV_{CC}$. When the bottom switch B turns on, the switch node SW1 drops to low and the boost capacitor $C_{BST1}$ is charged through diode $D_{BST1}$ from $DRV_{CC}$. When the top switch D turns on, the switch node SW2 rises to $V_{OUT}$ and the BOOST2 pin rises to approximately $V_{OUT} + DRV_{CC}$. When the bottom switch C turns on, the switch node SW2 drops to low and the boost capacitor $C_{BST2}$ is charged through diode DBST2 from $DRV_{CC}$. The boost capacitors $C_{BST1}$ and $C_{BST2}$ need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The low leakage Schottky diodes $D_{BST1}$ and $D_{BST2}$ must be able to handle the top driver current. Due to the large duty cycle and short on-time of BG1/BG2 when $V_{IN}$ is close to $V_{OUT}$, the pulse current on $D_{BST1}$ and $D_{BST2}$ could be higher than 100mA. It is suggested that the current capability of $D_{BST1}$ and $D_{BST2}$ higher than 100mA. The $D_{BST1}$ reverse breakdown voltage must be greater than $V_{IN}$ and $D_{BST1}$ reverse breakdown voltage must be greater than $V_{OUT}$.

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### $DRV_{CC}$ Regulators and $EXTV_{CC}$

The LTC7878 features a P-channel MOSFET LDO that supplies power to $DRV_{CC}$ from the $V_{IN}$ supply. $DRV_{CC}$ powers the gate drivers and most of the LTC7878's internal circuitry. The linear regulator regulates the voltage at the $DRV_{CC}$ pin to 7V when $V_{IN}$ voltage is greater than 7V. $EXTV_{CC}$ connects to $DRV_{CC}$ through another P-channel MOSFET LDO and can also regulate the $DRV_{CC}$ to 7V. LTC7878 internally choose the efficient LDO between $V_{IN}$ and $EXTV_{CC}$ to reduce the IC temperature. Both LDOs can supply the driver current and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7878 to be exceeded. The $DRV_{CC}$ current, which is dominated by the gate charge current, may be supplied by the linear regulator either from $V_{IN}$ or from $EXTV_{CC}$. Power dissipation for the IC in this case is highest and is equal to ($V_{IN}$ or $EXTV_{CC}$) • $I_{DRVCC}$. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics table. For example, the LTC7878 $DRV_{CC}$ current is 40mA from a 12V~60V $V_{IN}$ supply and no $EXTV_{CC}$ supply, the worst-case junction temperature at room temperature can be calculated by:

$$T_J = 25°C + (40mA)(60V)(34°C/W) = 106.6°C$$