Product/Process Change Notice - PCN 22_0065 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: Data Sheet Revision for AD9543/AD9545/AD9546

Publication Date: 08-Aug-2022

Effectivity Date: 10-Nov-2022 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

In I2C Mode Specifications table, the SCL/SDA Fall Time, tF entry: In the Test Conditions/Comments column, the following is introduced: Min specification requires configuring SDIO/SDA pin for low drive strength (bit 7 in register 0x0109 set to 1).

In I2C Mode Specifications table, the Data Hold Time, tHD;DAT entry: In the Test Conditions/Comments column, the following is introduced: Not compliant with the I2C specification of 0 µs min, 0.9 µs max in fast mode

Reason For Change:

Adding Test Conditions/Comments for certain I2C timing entries.

Impact of the change (positive or negative) on fit, form, function & reliability:

These changes do not have any impact on fit, form, function or reliability.

Summary of Supporting Information:

Changes in this PCN will be reflected in the AD9543 and AD9546 data sheet rev A and in the AD9545 data sheet rev D.

Supporting Documents

Attachment 1: Type: Detailed Change Description

ADI_PCN_22_0065_Rev_-_AD9543_AD9545_AD9546 I2C_PCN_proposed_changes_20220209b.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas:	**Europe:**	**Japan:**	**Rest of Asia:**
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (6)				
AD9543 / AD9543BCPZ	AD9543 / AD9543BCPZ-REEL7	AD9545 / AD9545BCPZ	AD9545 / AD9545BCPZ-REEL7	AD9546 / AD9546BCPZ
AD9546 / AD9546BCPZ-REEL7				

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	08-Aug-2022	10-Nov-2022	Initial Release.

Data Sheet Revision of the AD9543/AD9545/AD9546 I2C Specification

The proposed changes to the Table 29 in the AD9545 rev C data sheet are emphasized below highlighted in yellow:

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					Valid for VDDIOA = 1.8 V, 2.5 V, and 3.3 V
Input Logic 1 Voltage	70			% of VDDIOA	
Input Logic 0 Voltage			0.3 × VDDIOA	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% of VDDIOA
Hysteresis of Schmitt Trigger Inputs	1.5			% of VDDIOA	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.2	V	I_{OUT} = 3 mA
Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	20 + 0.1 × C_B		250	ns	10 pF ≤ C_B ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL/SDA Rise Time, t_R	20 + 0.1 × C_B		300	ns	
SCL/SDA Fall Time, t_F	20 + 0.1 × C_B		300	ns	Min specification requires configuring SDIO/SDA pin for low drive strength (bit 7 in register 0x0109 set to 1)
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	Not compliant with the I²C specification of 0 µs min, 0.9 µs max in fast mode
Capacitive Load for Each Bus Line, C_B			400	pF	

Reasons for the proposals:

t_F: Fall time of both SDA and SCL signals

The AD9545 t_f range is 20 + 0.1C_b ns min to 300 ns max, which supports the I2C specification of the same range in fast mode. We measured 18.6 ns fall time when the AD9545 generates ACK, which does not meet the 20+0.1C_b ns min specification. We saw that lowering the drive strength of the AD9545 SDIO/SDA pin (bit 7 of register 0x109 set to 1) increases the fall time to 54 ns. The customer that found this accepted this approach.

t_R: Rise time for both SDA and SCL signals

I looked at the SDA rise time and it was 194ns, well within the data sheet specification range. I do not believe we should modify this specification entry.

SCL being generated by the controller does not make sense to check and specify.

$t_{HD;DAT}$: Data hold time for I2C-bus devices

The AD9545 $t_{HD;DAT}$ min is 100 ns, which does not meet the I2C specification of 0 µs min for both standard and fast modes. Also, the I2C specification has 3.45 µs max in standard mode and 0.9 µs in fast mode. AD9545 does not have any max value specified.