Product/Process Change Notice - PCN 22_0013 Rev. -

Analog Devices, Inc. One Analog Way, Wilmington, MA 01887

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: ADRF5547 ESD Sensitivity Specification and Data Sheet Change

Publication Date: 23-Mar-2022

Effectivity Date: 25-Jun-2022 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

The ESD protection circuits at RFout, VDD1 VDD2, BP and PD pins are changed for improved HBM robustness. The ESD-HBM specification of 1000V is kept the same. ESD-CDM specification is changed from 1250V to 500V.

Reason For Change:

Marginality on ESD-HBM robustness has been observed on various process lots after the manufacturing release of the part. The design is improved to have higher margin for ESD-HBM specification but lower ESD-CDM performance.

Impact of the change (positive or negative) on fit, form, function & reliability:

This change will have no impact on the electrical performance, form, fit, or function of the device.

Product Identification *(this section will describe how to identify the changed material)*

Changed material identified by the LOT# in the device branding/marking.

Summary of Supporting Information:

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.
New ESD specification is given in rev B revision of the Product Data Sheet. See attached.

Supporting Documents

Attachment 1: Type: Qualification Results Summary

ADI_PCN_22_0013_Rev_-_ADRF5547-Qualification Results.pdf

Attachment 2: Type: Revised Datasheet Specification

ADI_PCN_22_0013_Rev_-_ADRF5547-RevB.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
ADRF5547 / ADRF5547BCPZN	ADRF5547 / ADRF5547BCPZN-R7	ADRF5547 / ADRF5547BCPZN-RL		

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	23-Mar-2022	25-Jun-2022	Initial Release.

Dual-Channel, 3.7 GHz to 5.3 GHz, Receiver Front End

Data Sheet **ADRF5547**

FEATURES

- Integrated dual-channel RF front end
  - 2-stage LNA and high power SPDT switch
  - On-chip bias and matching
  - Single-supply operation
- Gain
  - High gain mode: 33 dB typical at 4.6 GHz
  - Low gain mode: 18 dB typical at 4.6 GHz
- Low noise figure
  - High gain mode: 1.6 dB typical at 4.6 GHz
  - Low gain mode: 1.6 dB typical at 4.6 GHz
- High channel to channel isolation
  - Between RxOUT-ChA and RxOUT-ChB: 45 dB typical
  - Between TERM-ChA and TERM-ChB: 53 dB typical
- Low insertion loss: 0.50 dB typical at 4.6 GHz
- High power handling at T_{CASE} = 105°C
  - Full lifetime
    - LTE average power (9 dB PAR): 40 dBm
  - Single event (<10 sec operation)
    - LTE average power (9 dB PAR): 43 dBm
- High OIP3: 31 dBm typical
- Power-down mode and low gain mode for LNA
- Low supply current
  - High gain mode: 86 mA typical at 5 V
  - Low gain mode: 36 mA typical at 5 V
  - Power-down mode: 12 mA typical at 5 V
- Positive logic control
- 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- Wireless infrastructure
- TDD massive multiple input and multiple output (MIMO) and active antenna systems
- TDD-based communication systems

FUNCTIONAL BLOCK DIAGRAM

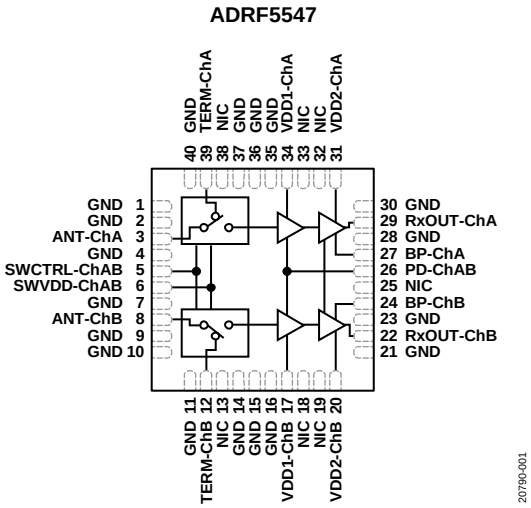


Figure 1.

GENERAL DESCRIPTION

The ADRF5547 is a dual-channel, integrated RF, front end multichip module designed for time division duplexing (TDD) applications that operates from 3.7 GHz to 5.3 GHz. The ADRF5547 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high power silicon, single-pole, double-throw (SPDT) switch.

In high gain mode, the cascaded, two-stage LNA and switch offer a low noise figure of 1.6 dB and high gain of 33 dB at 4.6 GHz with an output third order intercept point (OIP3) of 31 dBm (typical).

In low gain mode, one stage of the two-stage LNAs is in bypass, providing 18 dB gain at lower current of 36 mA. In power-down mode, the LNAs are turned off and the device draws 12 mA.

In transmit operation, when RF inputs are connected to a termination pin (TERM-ChA or TERM-ChB), the switch provides a low insertion loss of 0.50 dB and handles long term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 40 dBm for full lifetime operation and 43 dBm for single event (<10 sec) LNA protection operation.

The device comes in an RoHS compliant, compact, 40-lead, 6 mm × 6 mm LFCSP.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

1/2022—Rev. A to Rev. B

Changes to Charge Device Model (CDM) Parameter, Table 2 5
Changes to Figure 8, Figure 9, Figure 11, and Figure 13 8
Changes to Figure 14 and Figure 15 9
Changes to Figure 16, Figure 17, Figure 19, and Figure 21 10
Changes to Figure 22 and Figure 23 11
Changes to Figure 24 12

6/2020—Rev. 0 to Rev. A

Changes to Theory of Operation Section 13
Changes to Applications Information Section and Figure 28 14

10/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, and SWVDD-ChAB = 5 V, SWCTRL-ChAB = 0 V or SWVDD-ChAB, BP-ChA = VDD1-ChA or 0 V, BP-ChB = VDD1-ChB or 0 V, PD-ChAB = 0 V or VDD1-ChA, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

Table 1

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		3.7		5.3	GHz
GAIN[1]	Receive operation at 4.6 GHz				
High Gain Mode			33		dB
Low Gain Mode			18		dB
GAIN FLATNESS[1]	Receive operation in any 100 MHz bandwidth				
High Gain Mode			0.6		dB
Low Gain Mode			0.2		dB
NOISE FIGURE[1]	Receive operation at 4.6 GHz				
High Gain Mode			1.6		dB
Low Gain Mode			1.6		dB
OUTPUT THIRD ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, two-tone output power = 8 dBm per tone at 1 MHz tone spacing				
High Gain Mode			31		dBm
Low Gain Mode			22		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)					
High Gain Mode			18		dBm
Low Gain Mode			6		dBm
INSERTION LOSS[1]	Transmit operation at 4.6 GHz		0.50		dB
CHANNEL TO CHANNEL ISOLATION[1]	At 4.6 GHz				
Between RxOUT-ChA and RxOUT-ChB	Receive operation		45		dB
Between TERM-ChA and TERM-ChB	Transmit operation		53		dB
SWITCH ISOLATION[1]					
ANT-ChA to TERM-ChA and ANT-ChB to TERM-ChB	Transmit operation, PD-ChAB = 0 V		20		dB
SWITCHING CHARACTERISTICS (T_{ON}, T_{OFF})					
	50% control voltage to 90%, 10% of RxOUT-ChA or RxOUT-ChB in receive operation		860		ns
	50% control voltage to 90%, 10% of TERM-ChA or TERM-ChB in transmit operation		800		ns
RF INPUT POWER AT ANT-CHA, ANT-CHB[1]	Receive operation, LTE average (9 dB PAR)			15	dBm
RECOMMENDED OPERATING CONDITIONS					
Bias Voltage Range	VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB, SWVDD-ChAB	4.75	5	5.25	V
Control Voltage Range[2]	SWCTRL-ChAB, BP-ChA, BP-ChB, PD-ChAB	0		V_{DD}	V
RF Input Power at ANT-ChA, ANT-ChB	SWCTRL-ChAB = 5 V, BP-ChA = BP-ChB = 0 V, PD-ChAB = 5 V, T_{CASE} = 105°C[2]				
	Continuous wave			40	dBm
	9 dB PAR LTE full lifetime average			40	dBm
	9 dB PAR LTE single event (<10 sec) average			43	dBm
Case Temperature Range (T_{CASE})[3]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[1, 3]					
	Receive operation			132	°C
	Transmit operation			134	°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
SWCTRL-ChAB, PD-ChAB					
Low (V_{IL})		0		0.7	V
High (V_{IH})[2]		1.4		V_{DD}	V
BP-ChA, BP-ChB					
Low (V_{IL})		0		0.3	V
High (V_{IH})[2]		1.0		V_{DD}	V
SUPPLY CURRENT (I_{DD})	VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB = 5 V per channel				
High Gain Mode			86		mA
Low Gain Mode			36		mA
Power-Down Mode			12		mA
Transmit Current (Switch)	SWVDD-ChAB = 5 V		4.3		mA
DIGITAL INPUT CURRENTS	SWCTRL-ChAB, PD-ChAB, BP-ChA, BP-ChB = 5 V per channel				
SWCTRL-ChAB			0.0004		mA
PD-ChAB			0.2		mA
BP-ChA, BP-ChB			0.4		mA

[1] See Table 5 and Table 6.
[2] V_{DD} (shown in the maximum column) is the voltage of the SWVDD-ChAB, VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB pins.
[3] Measured at the exposed pad (EPAD).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage	
VDD1-ChA, VDD1-ChB, VDD2-ChA, VDD2-ChB	7 V
SWVDD-ChAB	5.4 V
Digital Control Input Voltage	
SWCTRL-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
BP-ChA, BP-ChB, PD-ChAB	−0.3 V to V_{DD}[1] + 0.3 V
RF Input Power (LTE Peak)	
Transmit	53 dBm
Receive	25 dBm
Temperature	
Storage	−65°C to +150°C
Reflow (Moisture Sensitivity Level (MSL) 3 Rating)	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	1 kV, Class 1C
Charge Device Model (CDM)	500 V, Class C2A

[1] V_{DD} is the voltage of the VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-40-15		
High Gain and Low Gain Mode	30	°C/W
Power-Down Mode	8.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

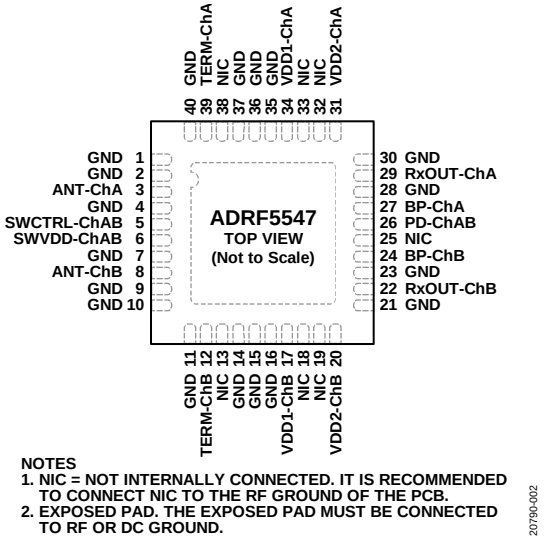


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 7, 9 to 11, 14 to 16, 21, 23, 28, 30, 35 to 37, 40	GND	Ground. See Figure 3 for the interface schematic.
3	ANT-ChA	RF Input to Channel A.
5	SWCTRL-ChAB	Control Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic.
6	SWVDD-ChAB	Supply Voltage for Switches on Channel A and Channel B. See Figure 7 for the interface schematic.
8	ANT-ChB	RF Input to Channel B.
12	TERM-ChB	Termination Output. This pin is the transmitter path for Channel B.
13, 18, 19, 25, 32, 33, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-ChB	Supply Voltage for Stage 1 LNA on Channel B. See Figure 5 for the interface schematic.
20	VDD2-ChB	Supply Voltage for Stage 2 LNA on Channel B. See Figure 5 for the interface schematic.
22	RxOUT-ChB	RF Output. This pin is the receiver path for Channel B. See Figure 4 for the interface schematic.
24	BP-ChB	Bypass Second Stage LNA of Channel B. See Figure 6 for the interface schematic.
26	PD-ChAB	Power-Down All Stages of LNA for Channel A and Channel B. See Figure 6 for the Interface schematic.
27	BP-ChA	Bypass Second Stage LNA of Channel A. See Figure 6 for the interface schematic.
29	RxOUT-ChA	RF Output. This pin is the receiver path for Channel A. See Figure 4 for the interface schematic.
31	VDD2-ChA	Supply Voltage for Stage 2 LNA on Channel A. See Figure 5 for the interface schematic.
34	VDD1-ChA	Supply Voltage for Stage 1 LNA on Channel A. See Figure 5 for the interface schematic.
39	TERM-ChA	Termination Output. This pin is the transmitter path for Channel A.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

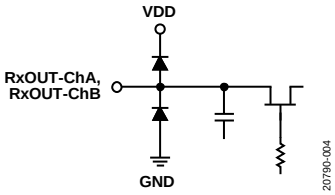


Figure 4. RxOUT-ChA and RxOUT-ChB Interface Schematic

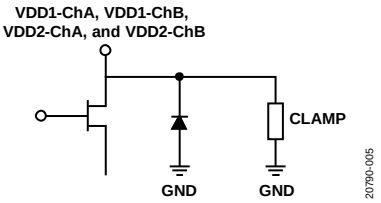


Figure 5. VDD1-ChA, VDD1-ChB, VDD2-ChA, and VDD2-ChB Interface Schematic

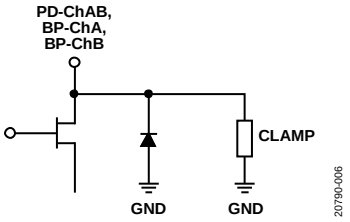


Figure 6. PD-ChAB, BP-ChA, and BP-ChB Interface Schematic

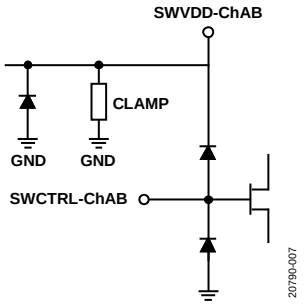


Figure 7. SWCTRL-ChAB, SWVDD-ChAB Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, HIGH GAIN MODE

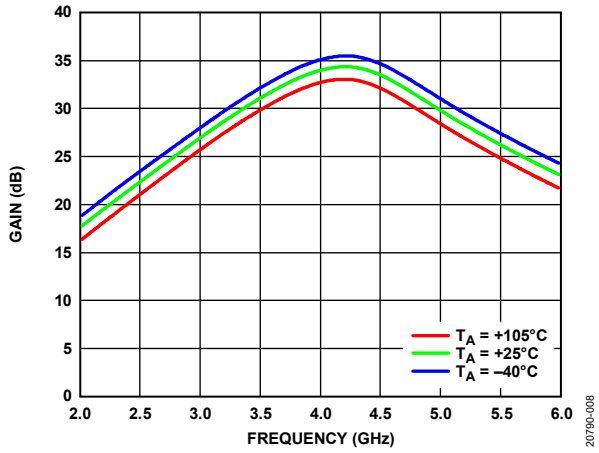


Figure 8. Gain vs. Frequency at Various Temperatures

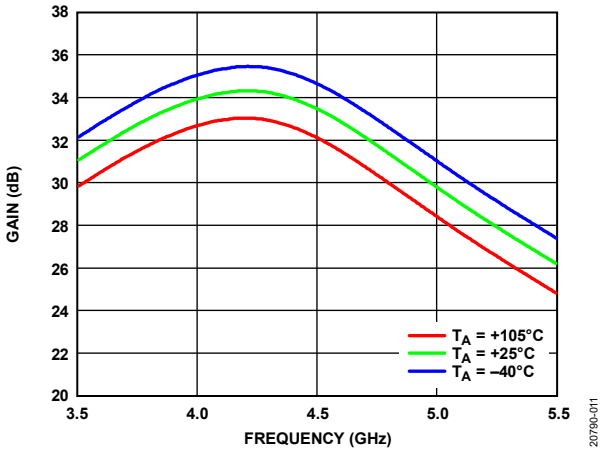


Figure 11. Gain vs. Frequency at Various Temperatures, 3.5 GHz to 5.5 GHz

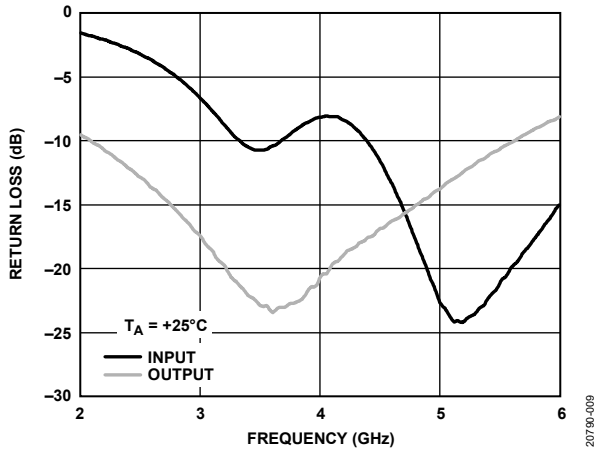


Figure 9. Return Loss vs. Frequency

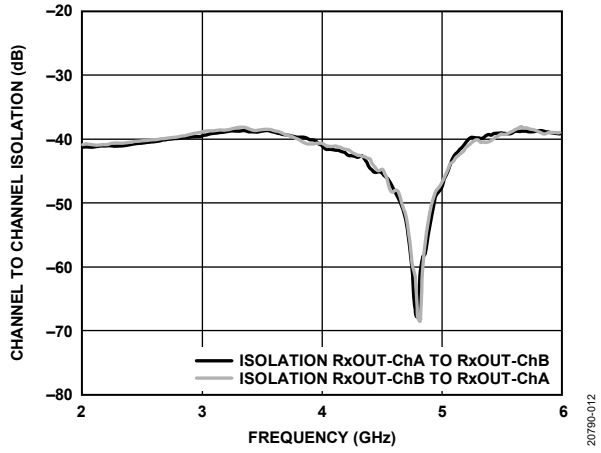


Figure 12. Channel to Channel Isolation vs. Frequency

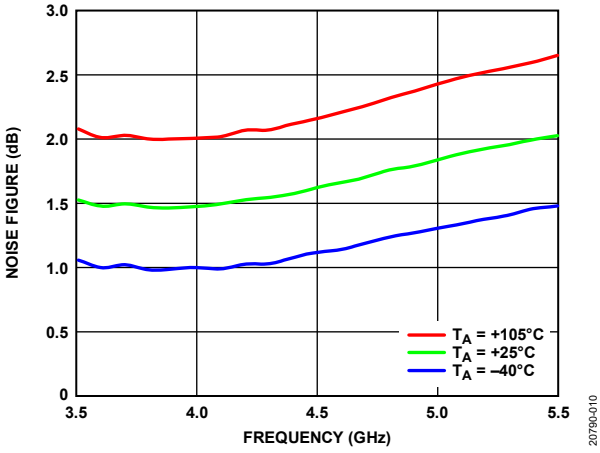


Figure 10. Noise Figure vs. Frequency for Various Temperatures

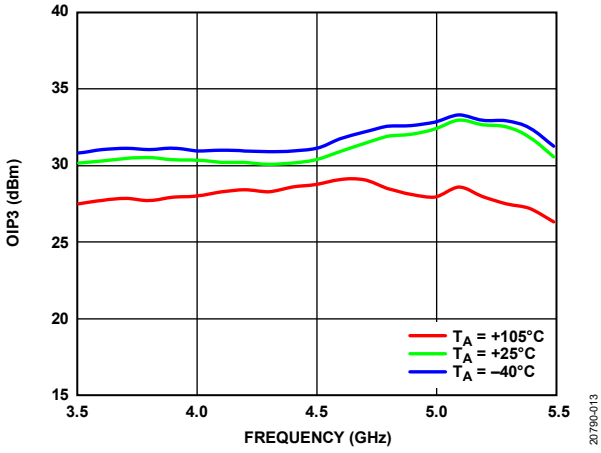


Figure 13. OIP3 vs. Frequency for Various Temperatures, 8 dBm Output Tone Power

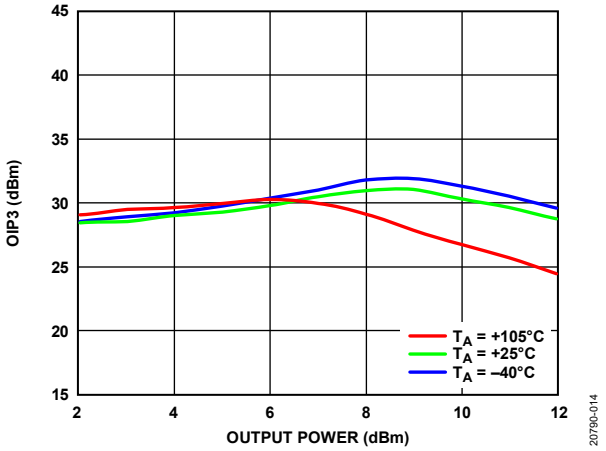


Figure 14. OIP3 vs. Output Power for Various Temperatures, 4.6 GHz

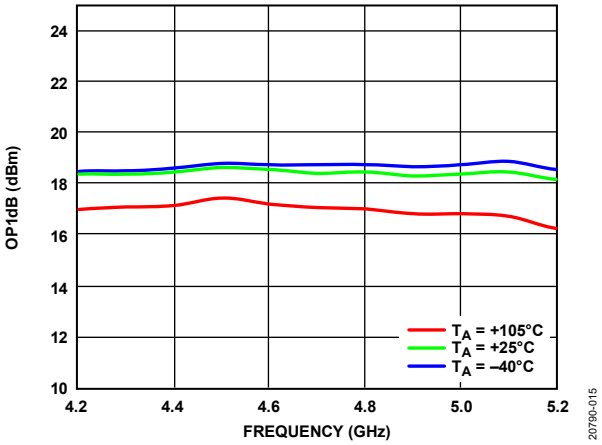


Figure 15. OP1dB vs. Frequency at Various Temperatures

RECEIVE OPERATION, LOW GAIN MODE

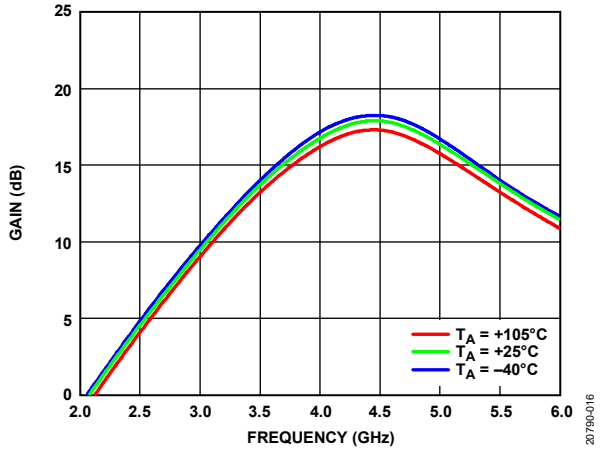


Figure 16. Gain vs. Frequency at Various Temperatures

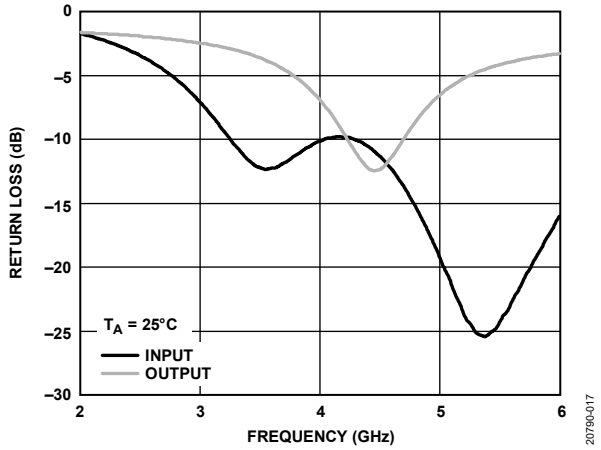


Figure 17. Return Loss vs. Frequency

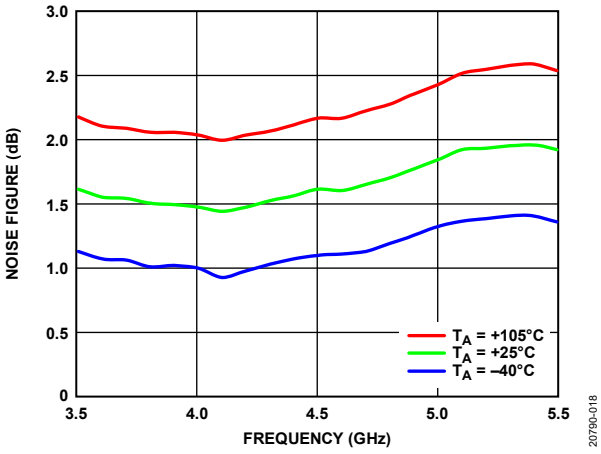


Figure 18. Noise Figure vs. Frequency at Various Temperatures

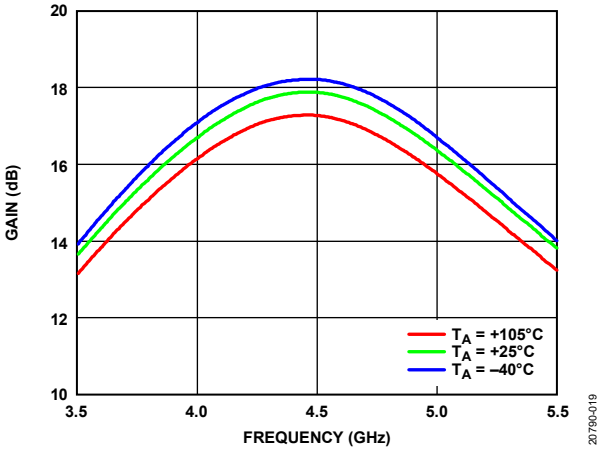


Figure 19. Gain vs. Frequency at Various Temperatures, 3.5 GHz to 5.5 GHz

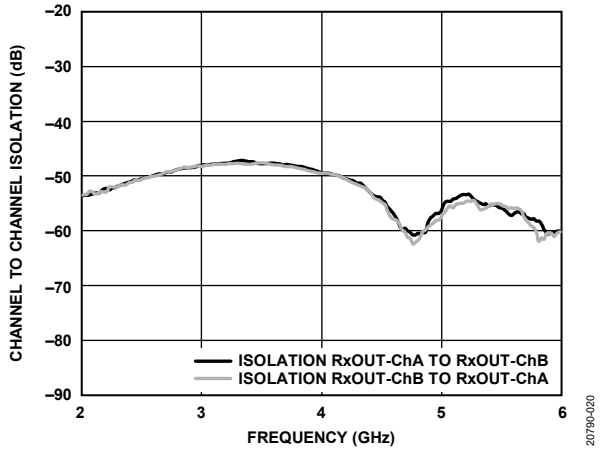


Figure 20. Channel to Channel Isolation vs. Frequency

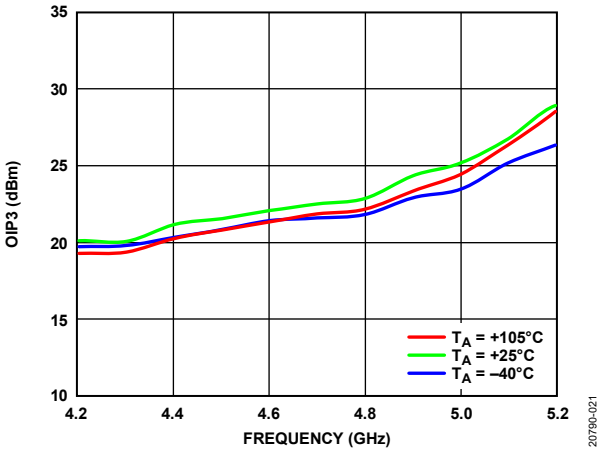


Figure 21. OIP3 vs. Frequency at Various Temperatures, –8 dBm Output Tone Power

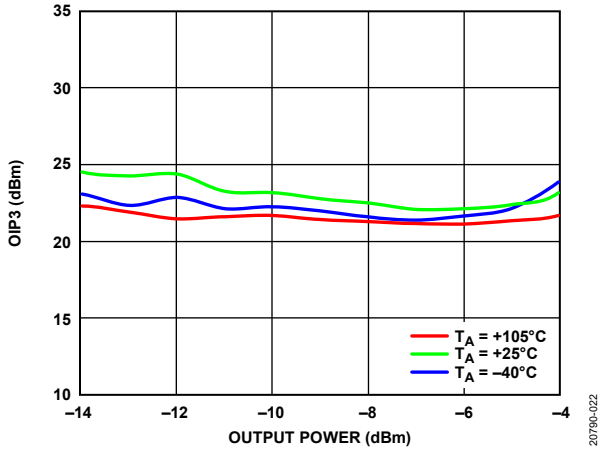


Figure 22. OIP3 vs. Output Power for Various Temperatures, 4.6 GHz

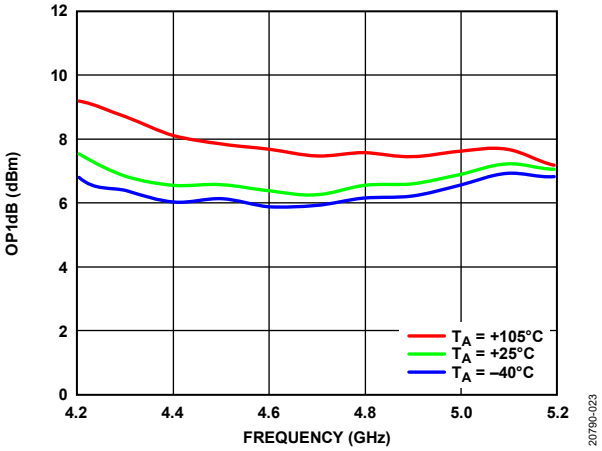


Figure 23. OP1dB vs. Frequency at Various Temperatures

TRANSMIT OPERATION

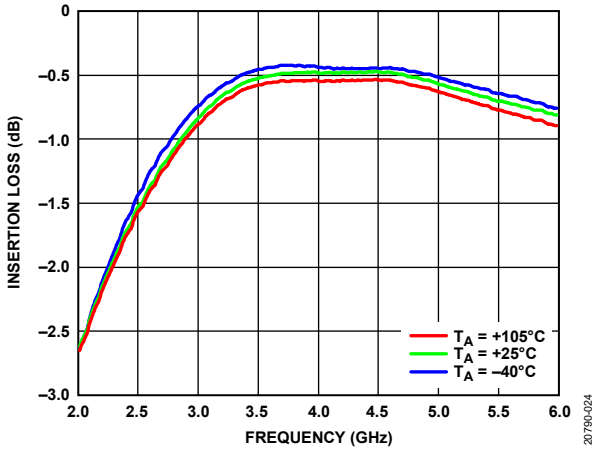


Figure 24. Insertion Loss vs. Frequency at Various Temperatures

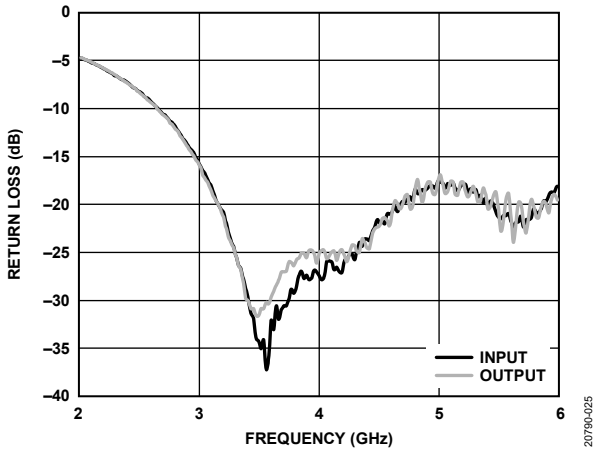


Figure 25. Return Loss vs. Frequency

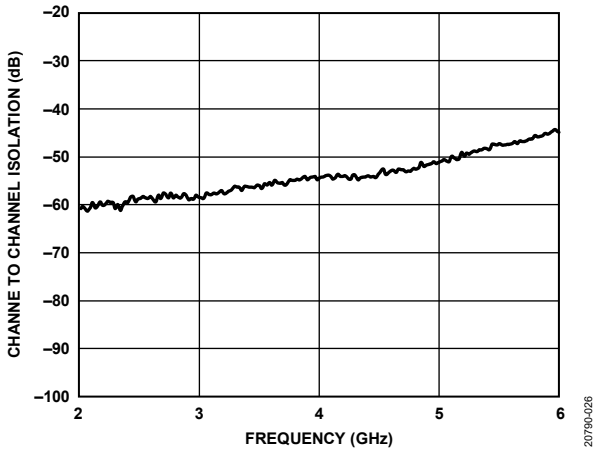


Figure 26. Channel to Channel Isolation vs. Frequency

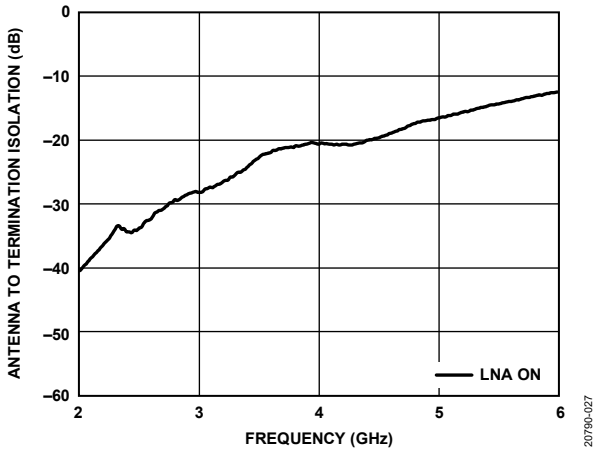


Figure 27. Antenna to Termination Isolation vs. Frequency

THEORY OF OPERATION

The ADRF5547 requires a positive supply voltage applied to VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB. Use bypassing capacitors on the supply lines to filter noise and use 300 Ω series resistors on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

SIGNAL PATH SELECT

When SWCTRL-ChAB is set to high, the ADRF5547 supports transmit operations. During this operation, when applying an RF input to ANT-ChA and ANT-ChB, the signal paths connect from ANT-ChA to TERM-ChA and from ANT-ChB to TERM-ChB.

When SWCTRL-ChAB is set to low, the ADRF5547 supports receive operations. During this operation, applying an RF input at ANT-ChA and ANT-ChB connects ANT-ChA to RxOUT-ChA and ANT-ChB to RxOUT-ChB.

Receive Operation

The ADRF5547 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 6.

When PD-ChAB is set to low, the LNA powers up and the user can select high gain mode or low gain mode. To select high gain mode, set BP-ChA or BP-ChB to low. To select low gain mode, set BP-ChA or BP-ChB to high.

When PD-ChAB is set to high, the ADRF5547 enters power-down mode. To select power-down high isolation mode, set BP-ChA or BP-ChB to low. To select power-down low isolation mode, set BP-ChA or BP-ChB to high.

BIASING SEQUENCE

To power up the ADRF5547, perform the following steps:

1. Connect GND to ground.
2. Power up VDD1-ChA, VDD2-ChA, VDD1-ChB, VDD2-ChB, and SWVDD-ChAB.
3. Power up SWCTRL-ChAB.
4. Power up PD-ChAB.
5. Power up BP-ChA and BP-ChB.
6. Apply an RF input signal to ANT-ChA and ANT-ChB.

To power down the ADRF5547, perform these steps in the reverse order.

Table 5. Truth Table: Signal Path

	Signal Path Select	
SWCTRL-ChAB	**Transmit Operation[1]**	**Receive Operation**
Low	Off	On
High	On	Off

[1] See the signal path descriptions in Table 6.

Table 6. Truth Table: Operation

Operation	PD-ChAB	BP-ChA, BP-ChB	Signal Path
Receive Operation			ANT-ChA to RxOUT-ChA, ANT-ChB to RxOUT-ChB
High Gain Mode	Low	Low	
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	

APPLICATIONS INFORMATION

To generate the evaluation PCB used in the application circuit shown in Figure 28, use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. Use 300 Ω series resistors on the BP-Chx and PD-ChAB digital control pins for glitch and overcurrent protection.

See the ADRF5547-EVALZ user guide for additional information on the evaluation board.

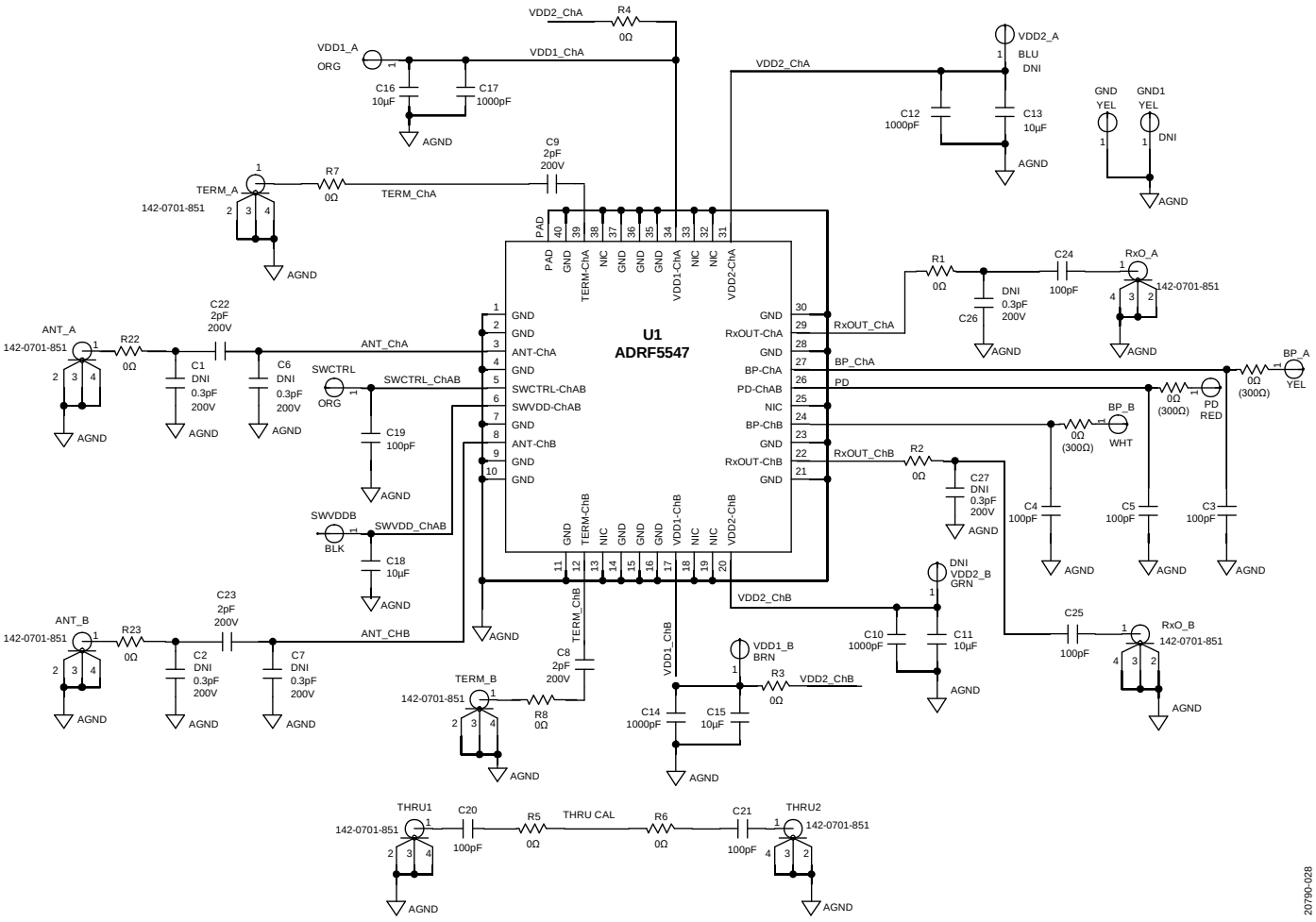
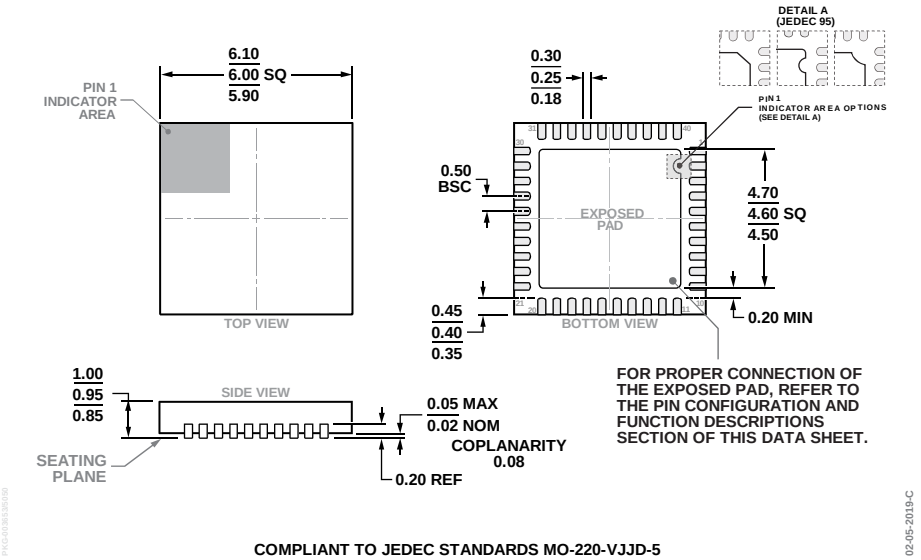


Figure 28. Application Circuit

OUTLINE DIMENSIONS



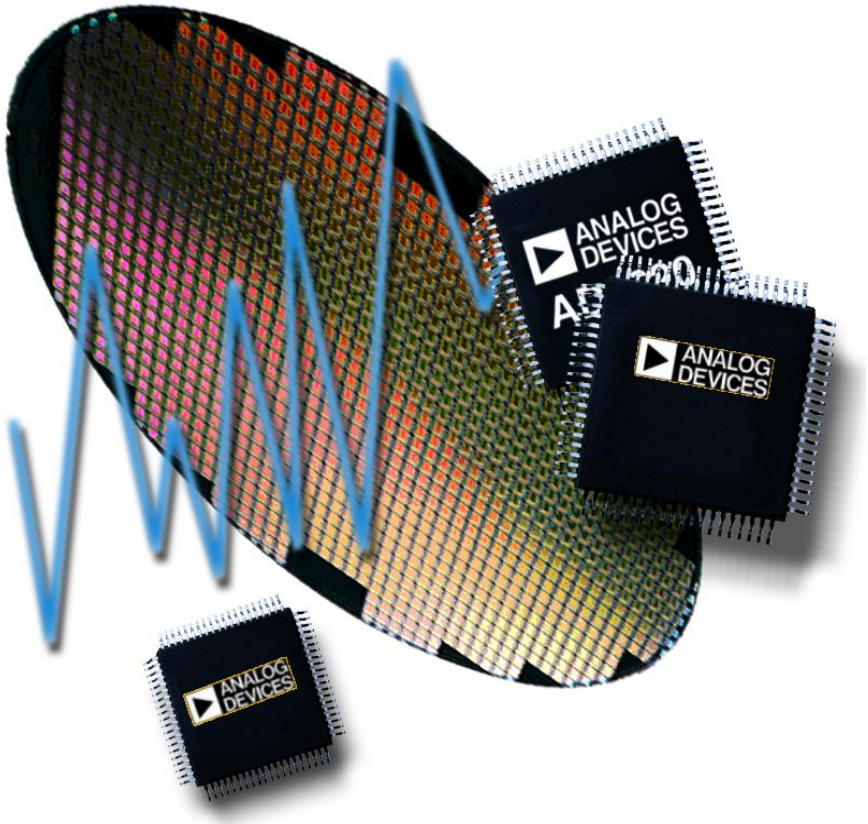
COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 29. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5547BCPZN	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5547BCPZN-R7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5547BCPZN-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5547-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.



Reliability Report

Report Title: ADRF5547 ESD Improvement Qualification

Report Number: 19198

Revision: A

Date: 14 March 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADRF5547 ESD improved product in a 40-LFCSP package. The ADRF5547 is a two channel 5G RF Front End MCM.

Table 1: ADRF5547 Product Characteristics

Die/Fab

Die Id	Die 1	Die 2	Die 3	Die 4
Die Size (mm)	2.11 x 1.89	1.27 x 1.07	2.11 x 1.89	1.27 x 1.07
Wafer Fabrication Process	0.18µm CMOS	0.25µm GaAs pHEMT	0.18µm CMOS	0.25µm GaAs pHEMT

Package/Assembly

Package	40-LFCSP
Body Size (mm)	6.00 x 6.00 x 0.95
Molding Compound	Epoxy
Die Attach	Conductive Epoxy
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1000 Hours	ADRF5545	Q14706.6	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130°C/85%RH 33.3 psia Biased 96 Hours	ADRF5545	Q14706.14	45	0
				Q14706.17	45	0
				Q14706.8	45	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-3	ADRF5547	Q14850.1	30	0
				Q16393.3	30	0
Temperature Cycling (TCT) [1]	JESD22-A104	-65°C/+150°C 1000 Cycles	ADRF5545	Q14706.11	45	0
				Q14706.19	45	0
				Q14706.2	45	0
Unbiased HAST (UHAST) [1]	JESD22-A118	130°C/85%RH 33.3 psia 96 Hours	ADRF5545	Q14706.13	45	0
				Q14706.16	45	0
				Q14706.21	45	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 3: 0.18µm CMOS Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	AEC-Q100-008	T_A=125°C 48 Hours	HMC8038WLP4CE	Q12190.EL1	667	0
				Q12190.EL2	667	0
				Q12190.EL3	667	0
High Temperature Operating Life (HTOL)	JESD22-A108	135°<Tj<150°C 2000 Hours	HMC8038WLP4CE	Q12190.HO1	77	0
				Q12190.HO2	77	0
				Q12190.HO3	77	0
		150°C<Tj<175°C Biased 1000 Hours	HMC1119LP4ME	Q11569.13	77	0
				Q11569.8	77	0
			HMC305SLP4E	Q12015.11	77	0
				Q12015.14	77	0
				Q12015.8	77	0
			HMC7992LP3DE	Q12018.11	77	0
			ADRF5545	Q14706.1	45	0
				Q14706.3	45	0
				Q14706.9	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1000 Hours	ADRF5130	Q12145.6	77	0
			ADRF5160	Q12144.11	77	0
				Q12144.5	77	0
				Q12144.8	77	0
			HMC1119LP4ME	Q11569.7	77	0
			HMC7992LP3DE	Q12018.3	77	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130°C/85%RH 33.3 psia Biased 96 Hours	HMC1119LP4ME	Q11569.11	77	0
			HMC305SLP4E	Q12015.13	77	0
				Q12015.9	77	0
			HMC540SLP3E	Q12017.7	77	0
				Q12017.9	77	0
			HMC7992LP3DE	Q12018.1	77	0
				Q12018.10	77	0
			HMC8038LP4CE	Q11991.10	77	0
				Q11991.9	77	0
			ADRF5545	Q14706.14	45	0
				Q14706.17	45	0
				Q14706.8	45	0
Low Temperature Operating Life (LTOL) [1]	JESD22-A108	-40°C Biased 1000 Hours	ADRF5020	Q12227.3	77	0
			ADRF5022	Q12229.4	77	0
			ADRF5041	Q12234.4	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Table 4: 0.25um GaAs PHEMT Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL)	JESD22-A108	150°C<Tj<175°C Biased 1000 Hours	ADRF5545	Q14706.1	45	0
				Q14706.3	45	0
				Q14706.9	45	0
Highly Accelerated Temperature and Humidity Stress Test (HAST) [1]	JESD22-A110	130°C/85%RH 33.3 psia Biased 96 Hours	ADRF5545	Q14706.14	45	0
				Q14706.17	45	0
				Q14706.8	45	0
			ADRF5539	Q14520.1	77	0
				Q14520.6	77	0
			ADRF5540	Q14515.2	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 5. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 5: ADRF5547 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	40-LFCSP	JS-002	1Ω, Cpkg	±500V	±750V	C2a
HBM	40-LFCSP	JS-001	1.5kΩ, 100pF	±1000V	±1250V	1C

Latch-Up Test Results

The ADRF5547 is built on dielectrically isolated wafer fabrication processes that are not susceptible to the latch-up phenomenon.

Approvals

Reliability Engineer: Adam Shaw

Additional Information

Data sheets and other additional information are available on Analog Devices' web site