



Product/Process Change Notice - PCN 21_0199 Rev. -

Analog Devices, Inc. One Analog Way, Wilmington, MA 01887

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: LTM2987 Datasheet Limit Change

Publication Date: 07-Sep-2021

Effectivity Date: 10-Dec-2021 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change:

Please be advised that Analog Devices has made minor changes to the LTM2987 product datasheet to facilitate improvement in manufacturing capability. The changes are shown on the attached page of the marked-up datasheets.

Electrical Characteristics table changes (page 4 of datasheet):

Full-Scale Output Voltage VFS_VDACP (DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_0) from 1.3 – 1.44V to 1.29 – 1.44V.

Full-Scale Output Voltage VFS_VDACP (DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_1) from 2.5 – 2.77V to 2.48 – 2.77V.

Integral Nonlinearity INL_VDACP removal of temperature range dot from specification.

Reason For Change:

To facilitate improvement in manufacturing capability.

Impact of the change (positive or negative) on fit, form, function & reliability:

This datasheet change does not impact the fit, form, function, or reliability of the LTM2987.

Product Identification *(this section will describe how to identify the changed material)*

The new silicon can be identified with date code and lot traceability identification.

Summary of Supporting Information:

Changes will be reflected on the new product datasheet. See changes on Electrical Characteristics table on page 4.

Comments

Changes will be reflected on the new product datasheet. See changes on Electrical Characteristics table on page 4.

Supporting Documents

Attachment 1: Type: Datasheet Specification Comparison

ADI_PCN_21_0199_Rev_-_LTM2987_Marked-up_Datasheet.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:
PCN_Americas@analog.com

Europe:
PCN_Europe@analog.com

Japan:
PCN_Japan@analog.com

Rest of Asia:
PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
LTM2987 / LTM2987BIY#PBF	LTM2987 / LTM2987CY#PBF	LTM2987 / LTM2987IY#PBF		

Appendix B - Revision History			
Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	07-Sep-2021	10-Dec-2021	Initial Release

Analog Devices, Inc.

DocId:8650 Parent DocId:None Layout Rev:8

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25^\circ\text{C}$. $V_{PWR} = V_{IN_SNS} = 12\text{V}$, V_{DD33} , REFP and REFM pins floating, unless otherwise indicated. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{UPDATE_ADC}	Update Time	Odd Numbered Channels in Current Sense Mode (Note 7)		160		ms
C_{IN_ADC}	Input Sampling Capacitance			1		pF
f_{IN_ADC}	Input Sampling Frequency			62.5		kHz
I_{IN_ADC}	Input Leakage Current	$V_{IN_ADC} = 0\text{V}$, $0\text{V} \leq V_{COMMONMODE} \leq 6\text{V}$, Current Sense Mode	●		± 0.5	μA
	Differential Input Current	$V_{IN_ADC} = 0.17\text{V}$, Current Sense Mode	●	80	250	nA
		$V_{IN_ADC} = 6\text{V}$, Voltage Sense Mode	●	10	15	μA

DAC Output Characteristics

N_VDACP	Resolution				10	Bits		
VFS_VDACP	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF	Buffer Gain Setting_0	●	1.3	1.38	1.44	V
		DAC Polarity = 1	Buffer Gain Setting_1	●	2.5	2.65	2.77	V
INL_VDACP	Integral Nonlinearity	(Note 8)			✗		±2	LSB
DNL_VDACP	Differential Nonlinearity	(Note 8)			●		±2.4	LSB
VOS_VDACP	Offset Voltage	(Note 8)			●		±10	mV
VDACP	Load Regulation (VDACPn - VDACMn)	VDACPn = 2.65V, IVDACPn Sourcing = 2mA				100		ppm/mA
		VDACPn = 0.1V, IVDACPn Sinking = 2mA				100		ppm/mA
	PSRR (VDACPn - VDACMn)	DC: 3.13V ≤ VDD33 ≤ 3.47V, VPWR = VDD33				60		dB
		100mV Step in 20ns with 50pF Load				40		dB
	DC CMRR (VDACPn - VDACMn)	-0.1V ≤ VDACMn ≤ 0.1V				60		dB
	Leakage Current	VDACPn Hi-Z, 0V ≤ VDACPn ≤ 6V			●		±100	nA
	Short-Circuit Current Low	VDACPn Shorted to GND			●	-10	-4	mA
	Short-Circuit Current High	VDACPn Shorted to VDD33			●	4	10	mA
COUT	Output Capacitance	VDACPn Hi-Z				10		pF
tS_VDACP	DAC Output Update Rate	Fast Servo Mode				500		μs

DAC Soft-Connect Comparator Characteristics

V_{OS_CMP}	Offset Voltage	$V_{DACPn} = 0.2\text{V}$	●	± 1	± 18	mV
		$V_{DACPn} = 1.3\text{V}$	●	± 2	± 26	mV
		$V_{DACPn} = 2.65\text{V}$	●	± 3	± 52	mV

Voltage Supervisor Characteristics

V_{IN_VS}	Input Voltage Range (Programmable)	$V_{IN_VS} = (V_{SENSEPN} - V_{SENSEMn})$	Low Resolution Mode	●	0	6	V
			High Resolution Mode	●	0	3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$		●	-0.1	0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
TUE_VS	Total Unadjusted Error	$2\text{V} \leq V_{IN_VS} \leq 6\text{V}$, Low Resolution Mode	●			± 1.25	% of Reading
		$1.5\text{V} < V_{IN_VS} \leq 3.8\text{V}$, High Resolution Mode	●			± 1.0	% of Reading
		$0.8\text{V} \leq V_{IN_VS} \leq 1.5\text{V}$, High Resolution Mode	●			± 1.5	% of Reading
t_{S_VS}	Update Period				12.21		μs