Product/Process Change Notice - PCN 21_0198 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: LTC2980 Datasheet Limit Change

Publication Date: 02-Sep-2021

Effectivity Date: 05-Dec-2021 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release

Description Of Change:

Please be advised that Analog Devices has made minor changes to the LTC2980 product datasheet to facilitate improvement in manufacturing capability. The changes are shown on the attached page of the marked-up datasheet.

Electrical Characteristics table changes (page 4 of datasheet):
Full-Scale Output Voltage VFS_VDACP (DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_0) from 1.32 – 1.44V to 1.29 – 1.44V.
Full-Scale Output Voltage VFS_VDACP (DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_1) from 2.53 – 2.77V to 2.48 – 2.77V.
Integral Nonlinearity INL_VDACP removal of temperature range dot from specification.

Reason For Change:

To facilitate improvement in manufacturing capability.

Impact of the change (positive or negative) on fit, form, function & reliability:

This datasheet change does not impact the fit, form, function, or reliability of the LTC2980.

Product Identification *(this section will describe how to identify the changed material)*

The new silicon can be identified with date code and lot traceability identification.

Summary of Supporting Information:

Changes will be reflected on the new product datasheet. See changes on Electrical Characteristics table on page 4.

Comments

Changes will be reflected on the new product datasheet. See changes on Electrical Characteristics table on page 4.

Supporting Documents

Attachment 1: Type: Datasheet Specification Comparison

ADI_PCN_21_0198_Rev_-_LTC2980_Marked-up_Datasheet.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (3)				
LTC2980 / LTC2980BIY#PBF	LTC2980 / LTC2980CY#PBF	LTC2980 / LTC2980IY#PBF		

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	02-Sep-2021	05-Dec-2021	Initial Release

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25} and REF pins floating, unless otherwise indicated. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
t_{UPDATE_ADC}	Update Time	Odd Numbered Channels in Current Sense Mode (Note 7)				160		ms
C_{IN_ADC}	Input Sampling Capacitance					1		pF
f_{IN_ADC}	Input Sampling Frequency					62.5		kHz
I_{IN_ADC}	Input Leakage Current	V_{IN_ADC} = 0V, 0V ≤ $V_{COMMONMODE}$ ≤ 6V, Current Sense Mode		●			±0.5	µA
	Differential Input Current	V_{IN_ADC} = 0.17V, Current Sense Mode		●		80	250	nA
		V_{IN_ADC} = 6V, Voltage Sense Mode		●		10	15	µA
DAC Output Characteristics								
N_V_{DACP}	Resolution					10		Bits
V_{FS_VDACP}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1	Buffer Gain Setting_0	●	~~1.32~~	1.38	1.44	V
			Buffer Gain Setting_1	●	~~2.53~~	2.65	2.77	V
INL_V_{DACP}	Integral Nonlinearity	(Note 8)		●			±2	LSB
DNL_V_{DACP}	Differential Nonlinearity	(Note 8)		●			±2.4	LSB
V_{OS_VDACP}	Offset Voltage	(Note 8)		●			±10	mV
V_{DACP}	Load Regulation (V_{DACPn} – V_{DACMn})	V_{DACPn} = 2.65V, I_{VDACPn} Sourcing = 2mA				100		ppm/mA
		V_{DACPn} = 0.1V, I_{VDACPn} Sinking = 2mA				100		ppm/mA
	PSRR (V_{DACPn} – V_{DACMn})	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}				60		dB
		100mV Step in 20ns with 50pF Load				40		dB
	DC CMRR (V_{DACPn} – V_{DACMn})	–0.1V ≤ V_{DACMn} ≤ 0.1V				60		dB
	Leakage Current	V_{DACPn} Hi-Z, 0V ≤ V_{DACPn} ≤ 6V		●			±100	nA
	Short-Circuit Current Low	V_{DACPn} Shorted to GND		●	–10		–4	mA
	Short-Circuit Current High	V_{DACPn} Shorted to V_{DD33}		●	4		10	mA
C_{OUT}	Output Capacitance	V_{DACPn} Hi-Z				10		pF
t_{S_VDACP}	DAC Output Update Rate	Fast Servo Mode				500		µs
DAC Soft-Connect Comparator Characteristics								
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V		●		±1	±18	mV
		V_{DACPn} = 1.3V		●		±2	±26	mV
		V_{DACPn} = 2.65V		●		±3	±52	mV
Voltage Supervisor Characteristics								
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	Low Resolution Mode	●	0		6	V
			High Resolution Mode	●	0		3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$		●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode				4		mV/LSB
		0V to 6V Range: Low Resolution Mode				8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode		●			±1.25	% of Reading
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode		●			±1.0	% of Reading
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode		●			±1.5	% of Reading
t_{S_VS}	Update Period					12.21		µs

1.29

2.48