Product/Process Change Notice - PCN 20_0203 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: Assembly Transfer of ADSP-21161N Products to STATS ChipPAC Korea

Publication Date: 30-Apr-2020

Effectivity Date: 02-Aug-2020 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

Assembly site for CSP_BGA moving from STATS ChipPAC Singapore (STA) to existing qualified site STATS ChipPAC Korea (SK3). Existing qualified BOM in SK3 will be used.

Reason For Change:

STATS ChipPAC Singapore issued a discontinuance notice to ADI to close their wirebonded products assembly by Dec 31, 2020.

ADI's assembly subcontractors manufacture our products using Analog Devices specified manufacturing flows, materials, process controls and monitors. This assures that our customers receive the same level of quality and reliability on products they receive from different manufacturing locations.

Impact of the change (positive or negative) on fit, form, function & reliability:

No impact on form, fit and function

Product Identification *(this section will describe how to identify the changed material)*

Parts assembled at SK3 will be identified by Assembly Lot number and Date Code

Summary of Supporting Information:

Qualification will be performed per AEC-Q100, Stress Test Qualification for Integrated Circuits. See attached Qualification Plan.

Supporting Documents

Attachment 1: Type: Qualification Plan

ADI_PCN_20_0203_Rev_-_Qualification Plan Summary for AEC Grade 1 CSP_BGA at SK3.pdf

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Attachment 2: Type: Delta Qualification Matrix

ADI_PCN_20_0203_Rev_-_ADSP-21161N_PCN-DeltaQualification-Matrix-ZVEI-4_1.xlsm

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Attachment 3: Type: Detailed Change Description

ADI_PCN_20_0203_Rev_-_ADSP-21161N BOM Change Summary.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (5)				
ADSP-21161N / AD90776Z	ADSP-21161N / AD91128Z	ADSP-21161N / ADSP-21161NCCAZ100	ADSP-21161N / ADSP-21161NKCAZ100	ADSP-21161N / ADSP-21161NYCAZ110

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	30-Apr-2020	02-Aug-2020	Initial Release.

Qualification Plan Summary for CSP_BGA at STATS ChipPAC Korea

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	3 x 77	Oct 2020
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	3 x 11	Oct 2020
Temperature Humidity Bias (THB)*	JEDEC *JESD22-A101*	3 x 77	Oct 2020
High Temperature Storage (HTS)	JEDEC *JESD22-A103*	1 x 45	Oct 2020
Unbiased Highly Accelerated Stress Test (UHAST)*	JEDEC *JESD22-A118*	3 x 77	Oct 2020

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.

ADSP-21161N BOM Change Summary

	Stats Singapore - STA *(From)*	**Stats Korea – SK3** *(To)*
D/A	Ablestik 2000 conductive	Ablestik 2000B conductive
Wire	Au / 1.0 mil	Au / 1.0 mil
EMC	G770	KE-G2280TS
Ball Composition	96.5Sn_3.0Ag_0.5Cu	96.5Sn_3.0Ag_0.5Cu