Product/Process Change Notice - PCN 18_0077 Rev. -

Analog Devices, Inc. Three Technology Way Norwood, Massachusetts 02062-9106

This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD623 Die Revision and Wafer Fabrication Process Change

Publication Date: 17-May-2018

Effectivity Date: 19-Aug-2018 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

1)Wafer Fabrication Process changed from CBCMOS to XFCB40.
2)AD623 layout has been revised to accommodate fab process change. This includes transistor layout and rerouting of circuitry.
3)Bond pad locations and bonding diagram has changed.

Reason For Change:

Migrating the AD623 to a newer process to ensure the quality and longevity of the supply chain.

Impact of the change (positive or negative) on fit, form, function & reliability:

No impact on fit, form, function and reliability when operated within data sheet specifications.

Product Identification *(this section will describe how to identify the changed material)*

Date codes starting 94 days after the publication of this PCN.

Summary of Supporting Information:

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Qualification Results Summary

ADI_PCN_18_0077_Rev_-_Qualification Results Summary.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas:	**Europe:**	**Japan:**	**Rest of Asia:**
PCN_Americas@analog.com	PCN_Europe@analog.com	PCN_Japan@analog.com	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (9)				
AD623 / AD623ARMZ	AD623 / AD623ARMZ-REEL	AD623 / AD623ARMZ-REEL7	AD623 / AD623ARZ	AD623 / AD623ARZ-R7
AD623 / AD623ARZ-RL	AD623 / AD623BRZ	AD623 / AD623BRZ-R7	AD623 / AD623BRZ-RL	

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	17-May-2018	19-Aug-2018	Initial Release.

Qualification Results Summary of AD623 Die Revision in SOIC_N Package

QUALIFICATION RESULTS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
High Temperature Operating Life (HTOL)	JEDEC *JESD22-A108*	**9x77**	**Pass**
Highly Accelerated Stress Test (HAST)*	JEDEC *JESD22-A110*	**9x77**	**Pass**
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	**9x77**	**Pass**
High Temperature Storage Life (HTSL)	JEDEC *JESD22-A103*	**3x77**	**Pass**
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	**3x11**	**Pass**
Latch-Up	JEDEC *JESD78*		**Pass**
Electrostatic Discharge *Human Body Model*	ESDA/JEDEC *JS-001*	**3/voltage**	**Pass 4000V**
Electrostatic Discharge *Field-Induced Charged Device Model*	JEDEC *JESD22-C101*	**3/voltage**	**Pass 1250V**

*These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: 1. Bake – 24 hours at 125ºC; 2. Soak – unbiased soak for 168 hours at 85C, 85%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260ºC.

Qualification Results Summary of AD623 Die Revision in MSOP Package

QUALIFICATION RESULTS			
TEST	**SPECIFICATION**	**SAMPLE SIZE**	**RESULTS**
High Temperature Operating Life (HTOL)	JEDEC *JESD22-A108*	**9x77**	**Pass**
Highly Accelerated Stress Test (HAST)*	JEDEC *JESD22-A110*	**9x77**	**Pass**
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	**9x77**	**Pass**
High Temperature Storage Life (HTSL)	JEDEC *JESD22-A103*	**3x77**	**Pass**
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	**3x11**	**Pass**
Latch-Up	JEDEC *JESD78*		**Pass**
Electrostatic Discharge *Human Body Model*	ESDA/JEDEC *JS-001*	**3/voltage**	**Pass 4000V**
Electrostatic Discharge *Field-Induced Charged Device Model*	JEDEC *JESD22-C101*	**3/voltage**	**Pass 1250V**

*These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: 1. Bake – 24 hours at 125ºC; 2. Soak – unbiased soak for 168 hours at 85C, 85%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260ºC.

Analog Devices, Inc. PCN Material Report (Proprietary Information)

Existing Material		Material Added		Material Removed	
GENERICNUMBER	MATERIALNUMBER	GENERICNUMBER	MATERIALNUMBER	GENERICNUMBER	MATERIALNUMBER
		AD623	AD623ARMZ		
		AD623	AD623ARMZ-REEL		
		AD623	AD623ARMZ-REEL7		
		AD623	AD623ARZ		
		AD623	AD623ARZ-R7		
		AD623	AD623ARZ-RL		
		AD623	AD623BRZ		
		AD623	AD623BRZ-R7		
		AD623	AD623BRZ-RL		