PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-IPC/12/7384
Dated 20 Jul 2012

Copper Wire Bonding Implementation on MLP package in Carsem Malaysia and Carsem China

Table 1. Change Implementation Schedule

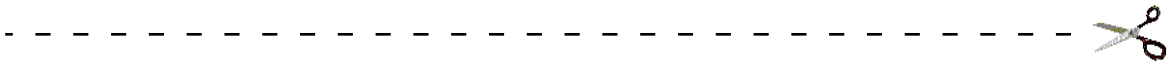
Forecasted implementation date for change	13-Jul-2012
Forecasted availability date of samples for customer	25-Sep-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	13-Jul-2012
Estimated date of changed product first shipment	19-Oct-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Package assembly material change
Reason for change	To follow the Company guidelines on bonding material implementation.
Description of the change	Pad structure (Top Metal) : Ni/Pd layer (3um Nickel / 0.3um Palladium thickness) is added Wire bonding : Pd/ Copper (1.3mils thickness)
Change Product Identification	Traced by a new internal part number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-IPC/12/7384**
Please sign and return to STMicroelectronics Sales Office	**Dated 20 Jul 2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Pioppo, Sergio Franco	Marketing Manager
Pioppo, Sergio Franco	Product Manager
Motta, Antonino	Q.A. Manager

ATTACHMENT TO PCN IPD-IPC/12/7384

WHAT*:*

"Pd/Cu wire bonding on Ni/Pd pad implementation" for BCD6S/ BCD6S_SOI solutions mounted in MLP package will be adopted.

The new production with Pd/copper wire is delivered by our subcontractor Carsem located in Malaysia (starting from Sep 2012) and will be supported from Carsem China (starting from Dec 2012).

The involved products are :

Product line	Commercial Product	Package description
UA2801	LNBH25LPQR	VFQFPN 4x4x1.0 24
UA2801	LNBH25PQR	VFQFPN 4x4x1.0 24
UA2801	LNBH25QTR/1L	VFQFPN 4x4x1.0 24
UA2901	LNBH26LPQR	VFQFPN 4x4x1.0 24
UA2901	LNBH26PQR	VFQFPN 4x4x1.0 24
UA2901	LNBH26SPQR	VFQFPN 4x4x1.0 24
UA3001	LNBH24LQTR	VFQFPN 5X5x1.0 32L
UA3001	LNBH24LQTR/1P	VFQFPN 5X5x1.0 32L
UM7601	LNBH23PQTR	VFQFPN 5X5x1.0 32L
UM7601	LNBH23TQTR	VFQFPN 5X5x1.0 32L
UM7601	LNBH23TQTR/SM	VFQFPN 5X5x1.0 32L
UM9001	LNBH23QTR	VFQFPN 5X5x1.0 32L
UM9001	LNBH23QTR/1B	VFQFPN 5X5x1.0 32L
UQ8701	LNBH23LQTR	VFQFPN 5X5x1.0 32L
UQ8701	LNBH23LQTR/1S	VFQFPN 5X5x1.0 32L
UJ7501	STOD13CM	VFDFPN 12L 3x3x0.55
UJ5801	STOD13ASTPUR	VFDFPN 12L 3x3x0.55
UJ7201	STOD13AMTPUR	VFDFPN 12L 3x3x0.55

WHY*:*

To comply with the Company requirements for bonding material implementation and to increase delivery flexibility.

HOW*:*

Please refer to the attached Reliability Reports related to Carsem Malaysia.

Three different test vehicles (UM90; UJ58; UJ75) have been checked to guarantee device performance, crossing Front End technologies (BCD6S/BCD6S_SOI) and Back End package assembly rules with Palladium/copper wire process.
Carsem China will be qualified taking into account relevant results got from Carsem Malaysia (same process, same materials and same equipments)

The new process (copper wire) can be traced by the internal part numbers on ST standard labels .

WHEN:
The production is scheduled to start in September, 2012 in Carsem Malaysia and in December 2012 in Carsem China.

For samples availability see table below.

cp	line	package	assy/tnf descr		Samples availability
LNBH25LPQR	UA2801	FPN 4X4	CARSEM S		10-Oct-12
LNBH25PQR	UA2801	FPN 4X4	CARSEM S		
LNBH25QTR/1L	UA2801	FPN 4X4	CARSEM S		
LNBH26LPQR	UA2901	FPN 4X4	CARSEM S		
LNBH26PQR	UA2901	FPN 4X4	CARSEM S		
LNBH26SPQR	UA2901	FPN 4X4	CARSEM S		
LNBH24LQTR	UA3001	FPN 5X5	CARSEM S		
LNBH24LQTR/1P	UA3001	FPN 5X5	CARSEM S		
LNBH23PQTR	UM7601	FPN 5X5	CARSEM S		
LNBH23TQTR	UM7601	FPN 5X5	CARSEM S		
LNBH23TQTR/SM	UM7601	FPN 5X5	CARSEM S		
LNBH23LQTR	UQ8701	FPN 5X5	CARSEM S		
LNBH23QTR/1B	UM9001	FPN 5X5	CARSEM S		
LNBH23LQTR/1S	UQ8701	FPN 5X5	CARSEM S		
LNBH23QTR	UM9001	FPN 5X5	CARSEM S		15-Jun-12
STOD13CM	UJ7501	FPN 3X3	CARSEM S		
STOD13ASTPUR	UJ5801	FPN 3X3	CARSEM S		
STOD13CM	UJ7501	FPN 3X3	CARSEM China		10-Oct-12
STOD13ASTPUR	UJ5801	FPN 3X3	CARSEM China		
STOD13AMTPUR	UJ7201	FPN 3X3	CARSEM S		25-Sep-12

Reliability Evaluation Report

Cu wires (1,3mils) - NiPd Pactech Process

Test Vehicles: ***LNBH23***

VFQFPN 5X5-32L Pitch 0.5 package
BCD6 Technology

General Information	
Product Line	*UM90*
P/N	*LNBH23QTR*
Product Group	*IPD*
Product division	*IND.& POWER CONV Handheld & Computer*
Package	*VFQFPN 5X5x1.0 32L Pitch 0.5*
Silicon Process technology	*BCD 6*

Locations	
Wafer fab	*Agrate + NiPd PACTECH Process*
Assembly plant	*Carsem S*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	21-May-2012	10	Alfio Rao - Giuseppe Giacopello	Giovanni Presti	First issue

This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Pd/Copper WIRE on Ni/Pd pad implementation.

Reliability evaluation on Cu wires (1,3MILS) using *NiPd PACTECH* process [Ni/Pd layer (3um Nickel / 0.3um Palladium thickness)] and assembled in FPN package.

Test Vehicles: LNBH23 in VFQFPN 5X5-32L Pitch 0.5 (BCD6).

UM90 – LNBH23 is the one of three TVs used during the reliability qualification.

3.2 Conclusion

The reliability results are positive.

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Device Characteristics

3.3 Device description

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.75 A), with integrated NMOS
- Selectable output current limit by external resistor
- Compliant with main satellite receiver systems specifications
- New accurate built-in 22 kHz tone generator suits widely accepted standards (patent pending)
- Fast oscillator start-up facilitates DiSEqC™ encoding
- Built-in 22 kHz tone detector supports bi-directional DiSEqC™ 2.0
- Very low-drop post regulator and high efficiency step-up PWM with integrated power NMOS allow low power losses
- Two output pins suitable to by-pass the output R-L filter and avoid any tone distortion (R-L filter as per DiSEqC™ 2.0 specs, see typ. application circuits)
- Overload and over-temperature internal protections with I²C diagnostic bits
- Output voltage and output current level diagnostic feedback by I²C bits
- LNB short circuit dynamic protection
- ± 4 kV ESD tolerant on output power pins

PowerSSO-24
(Exposed pad)

QFN32 (5 x 5 mm.)
(Exposed pad)

Description

Intended for analog and digital satellite receivers/sat-TV, sat-PC cards, the LNBH23 is a monolithic voltage regulator and interface IC, assembled in PowerSSO-24 ePAD and QFN32 (5 x 5 mm.) ePAD, specifically designed to provide the 13/18 V power supply and the 22 kHz tone signalling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

3.4 Construction note

	P/N: LNBH23QTR
Wafer/Die fab. information	
Wafer Fab Man. Location	AGRATE + *NiPd PACTECH* process
Technology	BCD 6
Die Finishing Back Side	Cr/NiV/Au
Die_Size	2130, 3260 micron
Bond pad met. Layers	NiPd
Assembly information	
Assembly site	Carsem S
Package description	VFQFPN 5X5x1.0 32L PITCH 0.5
Molding compound	Epoxy ECOPACK2
Die attach material	Loctite QMI519
Wires bonding materials/diameters	Cu 1,3 MILS
Final testing information	
Testing location	CARSEM S
Tester	ASL1000
Test program	LNBH23

4 TESTS RESULTS SUMMARY

4.1 Test vehicle

P/N: LNBH23QTR

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line
1	503894611U	sgc*engc0703	HY42*UM90XXA	VFQFPN 5X5x1.0 32L PITCH 0.5	UM90

4.2 Test plan and results summary

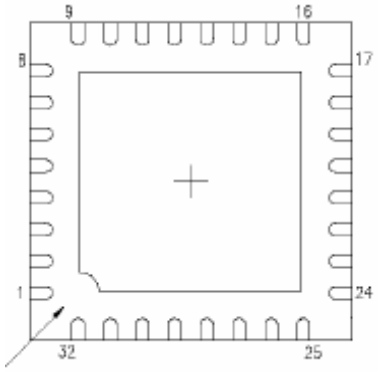
P/N: LNBH23QTR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 150℃	45	168 h	0/45	
					500 h	0/45	
					1000 h	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta= 85℃ Rh= 85% Oven Reflow @ Tpeak= 260℃ 3 times	300	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta= 121℃	77	168 h	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	

5 ANNEXES

5.1 Device details

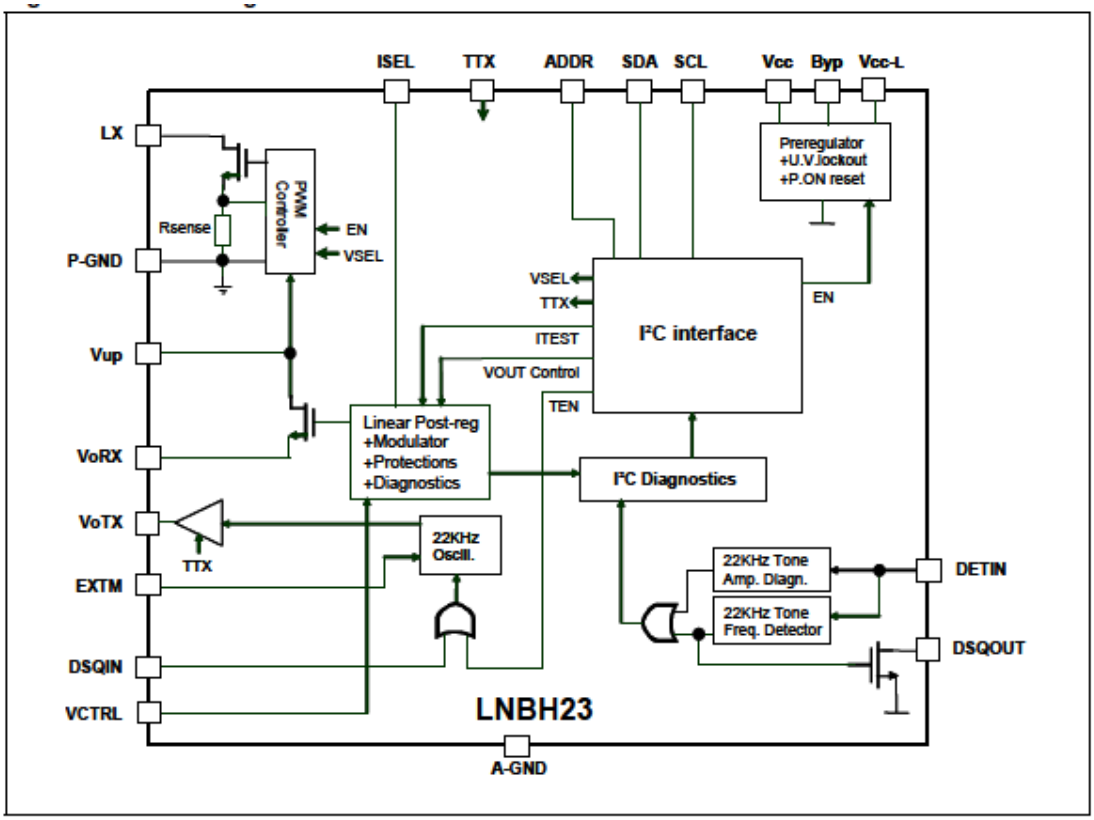
5.1.1 Pin connection



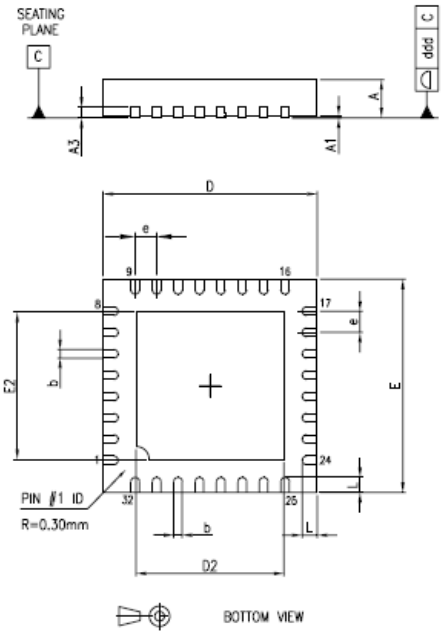
Pin description

Pin n° for QFN32	Pin n° for PSSO-24	Symbol	Name	Function
19	17	V_{CC}	Supply input	8 to 15 V IC DC-DC power supply.
18	16	V_{CC-L}	Supply input	8 to 15 V analog power supply.
4	6	LX	N-MOS drain	Integrated N-Channel power MOSFET drain.
27	22	V_{UP}	Step-Up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor.
21	19	V_{oRX}	LDO output port	Output of the integrated low drop linear post-regulator. See truth tables for voltage selections and description.
22	20	V_{oTX}	Output port for 22 kHz tone TX	TX Output to the LNB. See truth tables for selection.
6	8	SDA	Serial data	Bi-directional data from/to I²C bus.
9	9	SCL	Serial clock	Clock from I²C bus.
12	12	DSQIN	DiSEqC input	This pin will accept the DiSEqC code from the main microcontroller. The LNBH23 will use this code to modulate the internally generated 22 kHz carrier. Set to ground if not used.
14	14	TTX	TTX enable	This pin can be used, as well as the TTX I²C bit of the system register, to control the TTX function enable before to start the 22 kHz tone transmission. Set floating or to GND if not used.
29	1	DETIN	Tone decoder input	22 kHz tone decoder Input, must be AC coupled to the DiSEqC 2.0 bus.
11	11	DSQOUT	DiSEqC output	Open drain output of the tone decoder to the main microcontroller for DiSEqC 2.0 data decoding. It is LOW when tone is detected on DETIN pin.
13	13	EXTM	External modulation	External modulation logic input pin which activates the 22 kHz tone output on the V_{oTX} pin. Set to ground if not used.
15	15	BYP	By-pass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
10	10	ADDR	Address setting	Two I²C bus addresses available by setting the Address pin level voltage. See address pin characteristics *Table 10*
28	23	ISEL	Current selection	The resistor "RSEL" connected between ISEL and GND defines the linear regulator current limit threshold by the equation: Imax(typ.)=10000/ RSEL.
30	2	VCTRL	Output voltage control	13V-18V linear regulator V_{oRX} switch control. To be used only with V_{SEL}=1. If VCTRL=1 or floating V_{oRX}=18.5V (or 19.5V if LLC=1). If VCTRL=0 than V_{oRX}=13.4V (LLC=either 0 or 1). Leave floating if not used. Do not connect to ground if not used.
5	7	P-GND	Power ground	DC-DC converter power ground.
Epad	Epad	Epad	Exposed pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.
20	18	A-GND	Analog ground	Analog circuits ground.
1, 2, 3, 7, 8, 16, 17, 23, 24, 25, 26, 31, 32	3, 4, 5, 21, 24	N.C.	Not connected	Not internally connected pins.

5.1.2 Block diagram



5.1.3 Package outline/Mechanical data



Dim.	(mm.)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.20		3.70
E	4.85	5.00	5.15
E2	3.20		3.70
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

5.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Reliability Evaluation Report

Cu wires (1,3mils) - NiPd Pactech Process

Test Vehicles: ***STOD13ASTPUR***

VFDFPN 12L 3x3x0.55 Pitch 0.45
BCD 6SOI technology

General Information	
Product Line	*UJ58*
P/N	*STOD13ASTPUR*
Product Group	*IPD*
Product division	*IND.& POWER CONV Handheld & Computer*
Package	*VFDFPN 12L 3x3x0.55 PITCH 0.45*
Silicon Process technology	*BCD 6SOI*

Locations	
Wafer fab	*AG8 + NiPd PACTECH Process*
Assembly plant	*Carsem S*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	5-July-2012	10	Alfio Rao	Giovanni Presti	

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2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Pd/Copper WIRE on Ni/Pd pad implementation.

Reliability evaluation on Cu wires (1,3MILS) using *NiPd PACTECH* process [Ni/Pd layer (3um Nickel / 0.3um Palladium thickness)] and assembled in FPN package.

Test Vehicles: STOD13ASTPUR in VFDFPN 12L 3x3x0.55 PITCH 0.45 (BCD 6SOI)

UJ5801 - STOD13ASTPUR is the one of three TVs used during the reliability qualification.

The test plan has been chosen following the product mission profile.

3.2 Conclusion

Current reliability results are positive. The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

STOD13AS

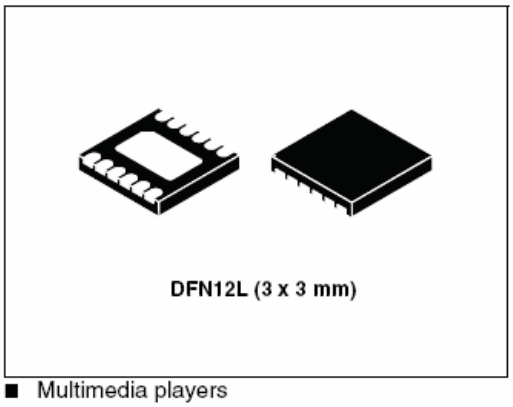
250 mA dual DC-DC converter
for powering AMOLED displays

Features

- Step-up and inverter converters
- Operating input voltage range from 2.5 V to 4.5 V
- Synchronous rectification for both DC-DC converters
- Minimum 250 mA output current
- 4.6 V fixed positive output voltage
- Programmable negative voltage by S_{WIRE} from -2.4 V to -6.4 V at 100 mV steps
- Typical efficiency: 85%
- Pulse skipping mode in light load condition
- 1.5 MHz PWM mode control switching frequency
- TDMA noise high immunity
- Enable pin for shutdown mode
- Low quiescent current in shutdown mode
- Soft-start with inrush current protection
- Overtemperature protection
- Temperature range: -40 °C to 85 °C
- True-shutdown mode
- Fast discharge outputs of the circuits after shutdown
- Short-circuit protection
- Package DFN12L (3 x 3 mm) 0.6 mm height

Applications

- Active matrix AMOLED power supply in portable devices
- Cellular phones
- Camcorders and digital still cameras



DFN12L (3 x 3 mm)

- Multimedia players

Description

The STOD13AS is a dual DC-DC converter for AMOLED display panels. It integrates a step-up and an inverting DC-DC converter making it particularly suitable for battery operated products, in which the major concern is overall system efficiency. It works in pulse skipping mode during low load conditions and PWM-MODE at 1.5 MHz frequency for medium/high load conditions. The high frequency allows the value and size of external components to be reduced. The Enable pin allows the device to be turned off, therefore reducing the current consumption to less than 1 µA. The negative output voltage can be programmed by an MCU through a dedicated pin which implements single-wire protocol. Soft-start with controlled inrush current limit, thermal shutdown, and short-circuit protection are integrated functions of the device.

Device summary

Order code	Positive voltage	Negative voltage	Package	Packaging
STOD13ASTPUR	4.6V	-2.4V to -6.4V	DFN12L (3 x 3mm)	3000 parts per reel

4.2 Construction note

	P/N: STOD13ASTPUR
Wafer/Die fab. information	
Wafer Fab Man. Location	AG8 + NiPd PACTECH process
Technology	BCD 6SOI
Process Family	SOIBCD6S_V2
Die Finishing Back Side	RAW SILICON
Die_Size	1610, 2235 micron
Assembly information	
Assembly site	CARSEM S
Package description	VFDFPN 12L 3x3x0.55 PITCH 0.45
Molding compound	Sumitomo G770H
Frame Material	Copper Olin 194
Die attach material	Loctite QMI519
Die pad size	104x75
Wires bonding materials/diameters	Cu 1.3 mils
Final testing information	
Testing location	CARSEM S

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

P/N: STOD13ASTPUR

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line
1	A202316	ENGC1703	RY26*UJ58AXA	VFDFPN 12L 3x3x0.55 PITCH 0.45	UJ58

5.2 Test plan and results summary

P/N: STOD13ASTPUR

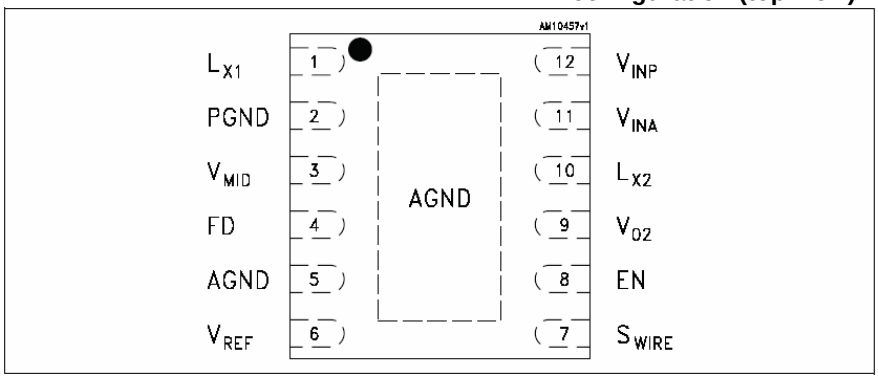
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTSL	N	JESD22 A-103	Ta = 150℃	45	168 h 500 h	0/45 0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta= 85℃ Rh= 85% Oven Reflow @ Tpeak= 260℃ 3 times	300	Final	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta= 121℃	77	168 h	0/77	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	77	100 cy 200 cy	0/77 0/77	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS: 4.6 V 6 V -10 V	77	168 h 500 h	0/77 0/77	

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Pin configuration (top view)

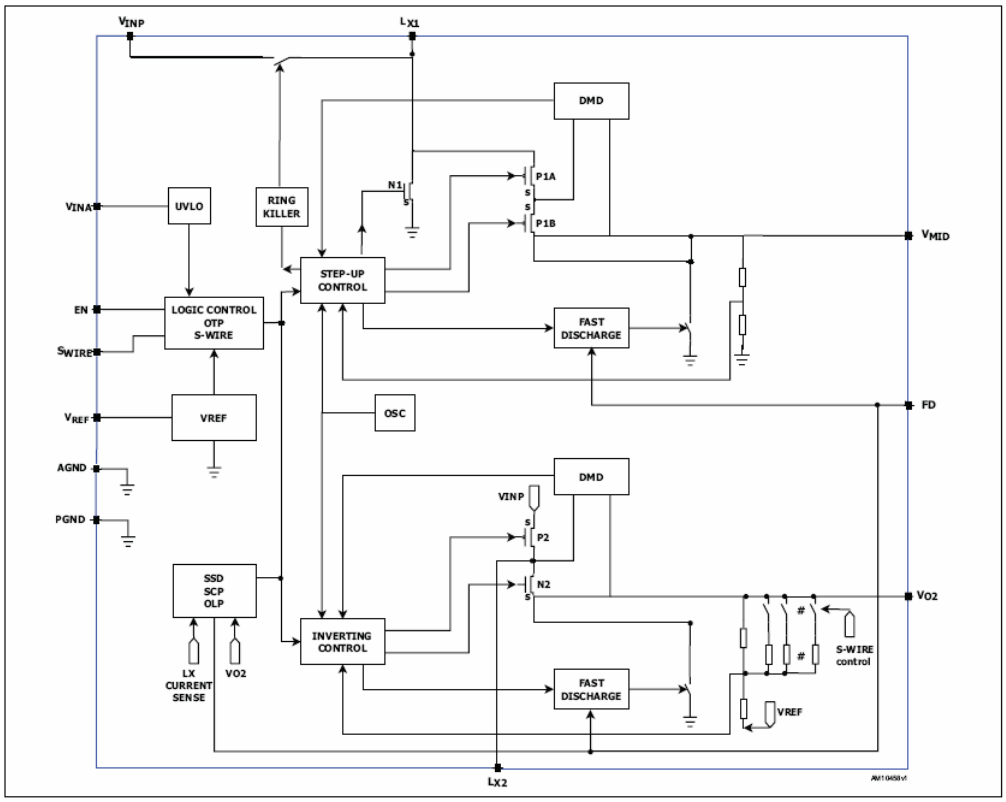


Pin description

Pin name	Pin n°	Description
Lx_1	1	Boost converter switching node
PGND	2	Power ground pin
V_{MID}	3	Boost converter output voltage
FD	4	Fast discharge control pin. When pulled LOW, the fast discharge after shutdown is active. When pulled HIGH, the fast discharge is OFF
AGND	5	Signal ground pin. This pin must be connected to the power ground layer
V_{REF}	6	Voltage reference output. 1 µF bypass capacitor must be connected between this pin and AGND
S_{WIRE}	7	Negative voltage setting pin
EN	8	Enable control pin. High = converter on; Low = converter in shutdown mode
V_{O2}	9	Inverting converter output voltage
Lx_2	10	Inverting converter switching node
$V_{IN\ A}$	11	Analogic input supply voltage
$V_{IN\ P}$	12	Power input supply voltage
	Exposed pad	Internally connected to AGND. Exposed pad must be connected to ground layers in the PCB layout in order to guarantee proper operation of the device

6.1.2 Block diagram

Block schematic

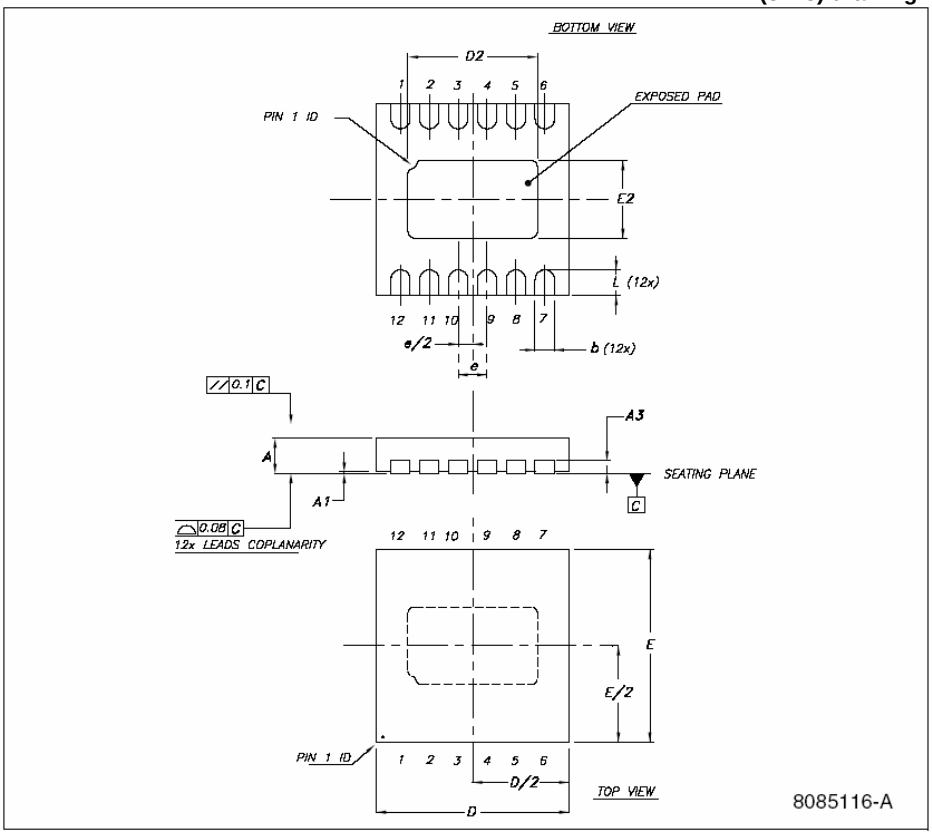


6.1.3 Package outline/Mechanical data

DFN12L (3 x 3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Typ.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.85	3	3.15	0.112	0.118	0.124
D2	1.87	2.02	2.12	0.074	0.080	0.083
E	2.85	3	3.15	0.112	0.118	0.124
E2	1.06	1.21	1.31	0.042	0.048	0.052
e		0.45			0.018	
L	0.30	0.40	0.50	0.012	0.016	0.020

DFN12L (3 x 3) drawing



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Evaluation Report

Cu wires (1,3mils) - NiPd Pactech Process

Test Vehicles: ***STOD13CMTPUR***

VFDFPN 12L 3x3x0.55 PITCH 0.45
BCD 6SOI technology

General Information	
Product Line	*UJ75*
P/N	*STOD13CMTPUR*
Product Group	*IPD*
Product division	*IND.& POWER CONV Handheld & Computer*
Package	*VFDFPN 12L 3x3x0.55 PITCH 0.45*
Silicon Process technology	*BCD 6SOI*

Locations	
Wafer fab	*AG8 + NiPd PACTECH Process*
Assembly plant	*Carsem S*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	5-Lug-2012	9	Alfio Rao	Giovanni Presti	First issue

This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Pd/Copper WIRE on Ni/Pd pad implementation.

Reliability evaluation on Cu wires (1,3MILS) using *NiPd PACTECH* process [Ni/Pd layer (3um Nickel / 0.3um Palladium thickness)] and assembled in FPN package.

Test Vehicles: STOD13CMTPUR in VFDFPN 12L 3x3x0.55 PITCH 0.45 (BCD 6SOI)

UJ75 - STOD13CMTPUR is the one of three TVs used during the reliability qualification.

3.2 Conclusion

Current reliability results are positive. The reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The STOD13CM is a dual DC/DC converter for AMOLED display panel. It integrates a step-up and an inverting DC-DC converter making it particularly suitable for battery operated products, in which the major concern is the overall system efficiency.

4.2 Construction note

	P/N: STOD13CMTPUR
Wafer/Die fab. information	
Wafer Fab Man. Location	AG8 + NiPd PACTECH Process
Technology	BCD 6SOI
Process Family	SOIBCD6S_V2
Die_Size	1610, 2235 micron
Assembly information	
Assembly site	CARSEM S
Package description	VFDFPN 12L 3x3x0.55 PITCH 0.45
Molding compound	Epoxy Ecopak2
Frame Material	Copper Olin 194
Die attach material	Loctite QMI519
Die pad size	104x75
Wires bonding materials/diameters	Cu 1.3 mils
Final testing information	
Testing location	CARSEM S

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

P/N: STOD13CMTPUR

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line
1	A148349A	#52723839	RY26*UJ75AXA	VFDFPN 12L 3x3x0.55 PITCH 0.45	UM75
Corner Lot HH	A148349A	#52723842	RY26*UJ75AXA	VFDFPN 12L 3x3x0.55 PITCH 0.45	UM75

5.2 Test plan and results summary

P/N: STOD13CMTPUR

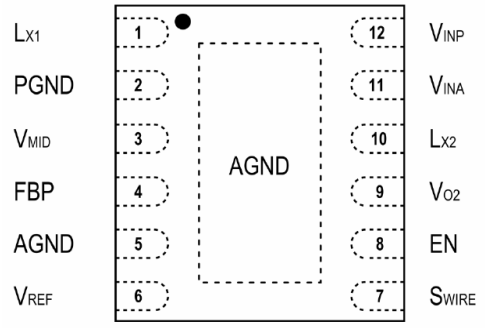
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		Note
						Lot 1	Corner Lot HH	
Die Oriented Tests								
HTSL	N	JESD22 A-103	Ta = 150℃	45	168 h	0/45	0/45	
					500 h	0/45	0/45	
Package Oriented Tests								
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta= 85℃ Rh= 85% Oven Reflow @ Tpeak= 260℃ 3 times	300	Final	Pass		
				100	Final		Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta= 121℃	77	168 h	0/77		
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	77	100 cy	0/77	0/77	
					200 cy	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, BIAS: 4.6 V 6 V -10 V	77	168 h	0/77		

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

STOD13CM **Pin Configuration**



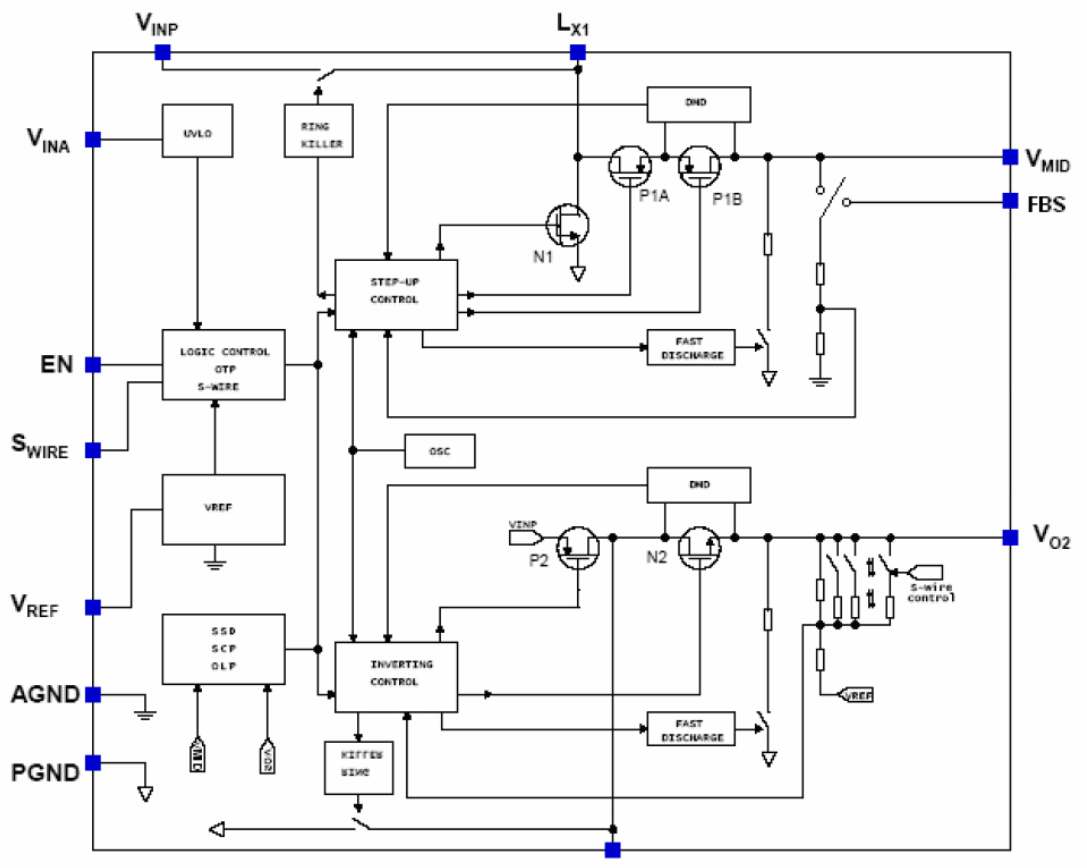
Pin Configuration (Top View)

Pin Description

Pin Name	Pin Number	Description
Lx_1	1	Boost Converter switching node.
PGND	2	Power Ground pin.
V_{MID}	3	Boost Converter output voltage.
FBS	4	Step-up Converter output voltage sense input. When connected to VMID at AMOLED panel enables external feedback, when connected to AGND enables internal feedback.
AGND	5	Signal ground pin. This pin must be connected to Power Ground layer.
V_{REF}	6	Voltage reference output. 1µF bypass capacitor must be connected between this pin and AGND.
S_{WIRE}	7	Negative voltage setting pin.
EN	8	Enable control pin. High = converter on; Low = converter in shutdown mode.
V_{O2}	9	Inverting Converter output voltage.
Lx_2	10	Inverting Converter switching node.
$V_{IN\ A}$	11	Analogic Input Supply Voltage.
$V_{IN\ P}$	12	Power Input Supply Voltage.
	EXPOSED PAD	Internally connected to AGND. Exposed pad must be connected to ground layers in the PCB layout in order to guarantee proper operation of the device.

6.1.2 Block diagram

Application Schematics **STOD13CM**



Block Schematics

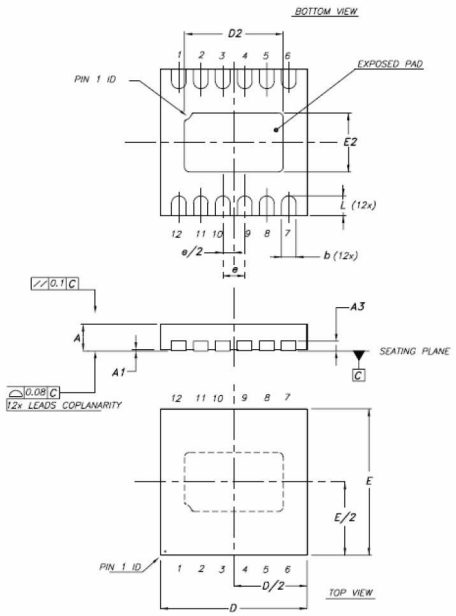
6.1.3 Package outline/Mechanical data

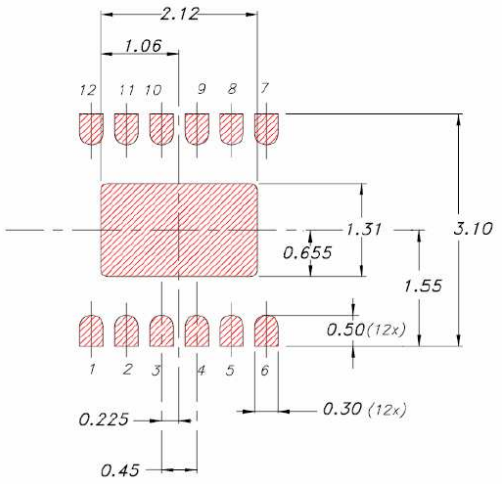
STOD13CM **Package Description**

Package Description

DFN12L 3x3x0.6 Mechanical Data

DFN12L (3 x 3 x 0.6 mm) mechanical data						
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	2.85	3	3.15	0.112	0.118	0.124
D2	1.87	2.02	2.12	0.074	0.080	0.083
E	2.85	3	3.15	0.112	0.118	0.124
E2	1.06	1.21	1.31	0.042	0.048	0.052
e		0.45			0.018	
L	0.30	0.40	0.50	0.012	0.016	0.020





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