PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/12/7129
Notification Date 03/09/2012

Improved design in CMOSF8H process for the M95512, 512 Kbit SPI bus EEPROM / industrial range

Table 1. Change Implementation Schedule

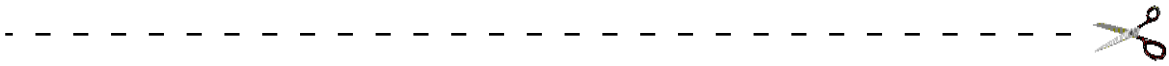
Forecasted implementation date for change	02-Mar-2012
Forecasted availabillity date of samples for customer	02-Mar-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	02-Mar-2012
Estimated date of changed product first shipment	08-Jun-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M95512 products family
Type of change	Product design change
Reason for change	Line up to state of art of design
Description of the change	Improved design of the CMOSF8H Process Technology
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Process Techno identifier is "8" for Improved design
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/12/7129**
Please sign and return to STMicroelectronics Sales Office	**Notification Date 03/09/2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
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Rodrigues, Benoit	Division Product Manager
Malbranche, Jean-Luc	Division Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

Improved design in CMOSF8H process for the M95512, 512 Kbit SPI bus EEPROM / industrial range

What is the change?

The **M95512, 512 Kbit SPI bus EEPROM** product family currently produced using the CMOSF8H process technology at ST Rousset (France) 8 inch wafer diffusion plant will undergo through an **improved design** leading to die size reduction (more compact layout).
This will also allow to offer **1.7 V** – 5.5 V ("-DF") Vcc range.
The M95512 with the improved design is functionally compatible to the current CMOSF8H version, as per datasheet (rev.15 – July 2011, here attached).

Following parameters will be updated in the revised datasheet (rev. 16):

AC characteristics (Industrial range 6):

- f_C Clock frequency: 10 MHz max when $V_{cc} \geq 2.5$ V (no more higher frequency when Vcc ≥ 4.5 V)

Concurrent to this change, the following production rationalization will follow:

- SO8N (Narrow, 150 mils) assembled on SHD line at ST Shenzhen will use 0.8 mil Copper wire (as introduced in PCN MMS-MMY/11/6929).
- MLP8 2x3 (UFDFPN) will change from small exposed pad (package code "MB") to large exposed pad (package code "MC"), PTN will be released in 2h/2012.
- WLCSP (Wafer Level Chip scale Package): Commercial Part Number will change from M95512-RCS6TP/K to M95512-DFCS6TP/K (with smaller dimensions, but compatible footprint), PTN will be released in 2h/2012.
- Wafer form will change from M95512-RKW20I/90 to M95512DFKW20I/90, PTN will be released 2h/2012

(See Appendix B for list of Commercial Part numbers)

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the improved design on the M95512 will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the M95512 with the improved design will ramp up from April 2012 and shipments can start from June 2012 onward (or earlier upon customer approval).

How will the change be qualified?

The M95512 with the improved design has been qualified using the standard ST Microelectronics Corporate Procedures for Quality and Reliability.

The **Qualification Report QRMMY1110** is available and included inside this document.

What is the impact of the change?

- **Form:** marking change: refer to **Device marking** paragraph
- **Fit:** no change
- **Function:** Max clock frequency change

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: The **Mask revision** identifier is "**B**" for the CMOSF8H **improved design** version, this identifier being "A" for the current CMOSF8H version.

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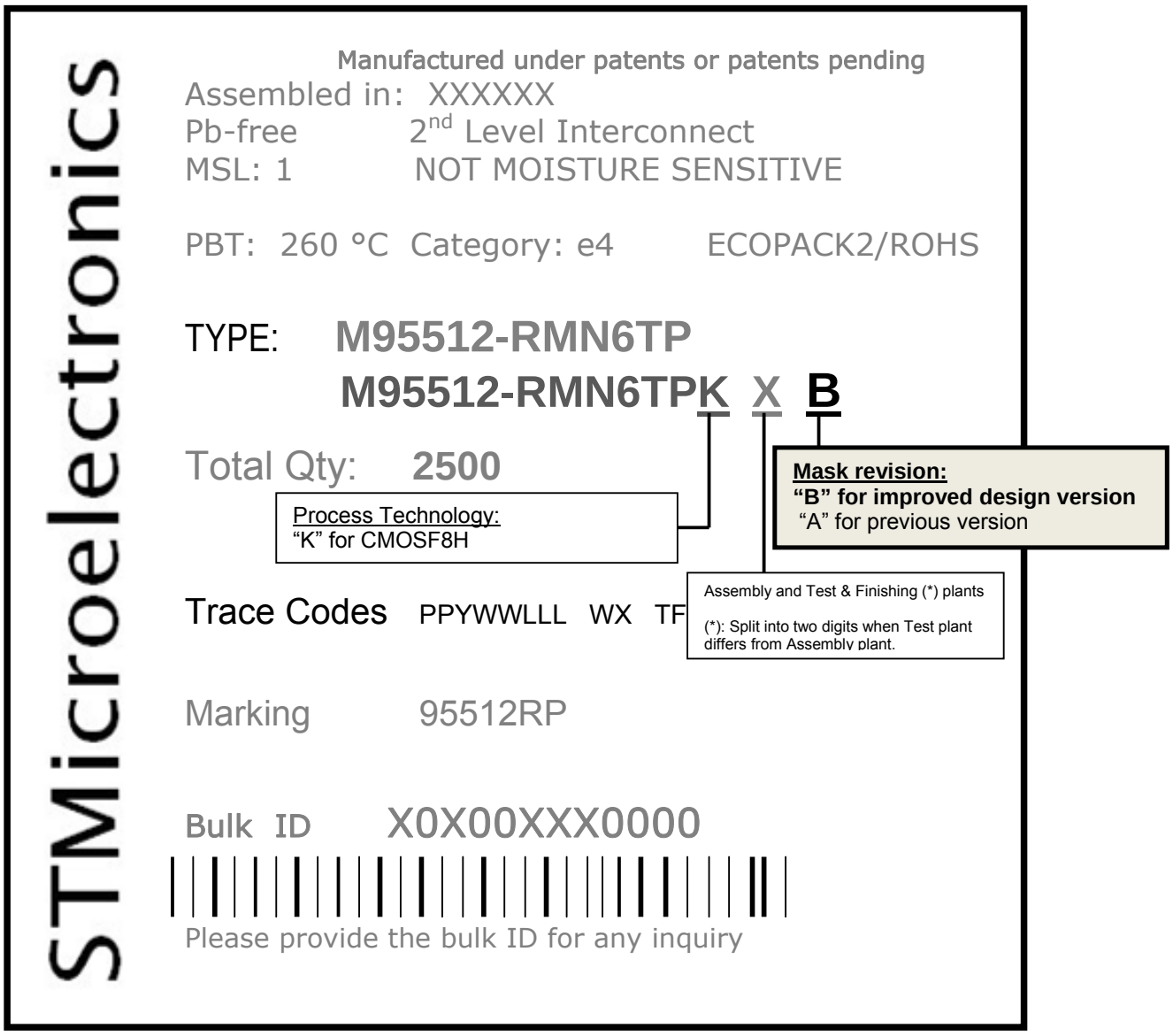
➔ *Example for M95512-RMN6TP*



How can the change be seen?

- DEVICE MARKING

On the DEVICE MARKING of the **SO8N** package, the difference is visible inside the trace code (PYWWT) where the last digit "T" for **Process Technology identifier** is "**8**" for the CMOSF8H **improved design** (Rev. B), this identifier being "K" for the current CMOSF8H (Rev. A).

	Improved design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
SO8N Example: M95512-RMN6TP	95512RP PYWW**8**	95512RP PYWW**K**

For **TSSOP8**, the difference is visible inside the product name: CMOSF8H **Improved design** (Rev. B) is ending by "**8**", current CMOSF8H (Rev. A) ending by "K".

	Improved design CMOSF8H (Rev. B)	Current CMOSF8H (Rev. A)
TSSOP8 Example: M95512-RDW6TP	512R**8** PYWW	512R**K** PYWW

Legend:

P = Assembly plant
Y = Year of Assembly last digit
WW = Assembly Week
T = Process Technology code/ Wafer Fab ID

Appendix A- Product Change Information

Product family / Commercial products:	M95512 products family
Customer(s):	All
Type of change:	Product design change
Reason for the change:	Line up to state of art of design
Description of the change:	Improved design of the CMOSF8H Process Technology.
Forecast date of the change: (Notification to customer)	Week 09 / 2012
Forecast date of Qualification samples availability for customer(s):	See details in next page
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The Qualification Report **QRMMY1110** is included inside this document
Marking to identify the changed product:	Process ID is “8” for improved F8H design
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Estimated date of first shipment:	Week 23 / 2012

Appendix B: Concerned Commercial Part Numbers:

- The following commercial part numbers will use the M95512 with the improved design:

Commercial Part Numbers	Samples availability
M95512-**R**DW6TP (*)	Week 12
M95512-**R**MN6P (*)	No samples in tube
M95512-**R**MN6TP (*)	Available
M95512-WDW6TP	Week 12
M95512-WMN6P	No samples in tubes
M95512-WMN6TP	Available

(*) Following product line rationalization, we recommend customer to use **–R** version (**1.8 V – 5.5 V**) when –W (2.5 V – 5.5 V) is used.
For instance, **M95512-RDW6TP should be preferred** to M95512-**W**DW6TP.

- The following part numbers will not be kept in production, replacement part numbers are:

Current Commercial Part Numbers	Replacement Commercial Part Numbers	Samples availability
M95512-**R**CS6TP/K	M95512-**DF**CS6TP/K	Available
M95512-**RMB**6TG	M95512-**DFMC**6TG	Week 23
M95512-**R**KW20I/90	M95512**DF**KW20I/90	Week 18

Appendix C: Qualification Report:

See following pages

QRMMY1110
Qualification report

Improved design / M95512-DF M95512-R M95512-W using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M95512-RMN6P M95512-RMN6TP M95512-WMN6P M95512-WMN6TP M95512-RDW6TP M95512-WDW6TP M95512-DFMN6TP M95512-DFDW6TP M95512-DFMC6TG M95512-DFCS6TP/K M95512-RKW20I/90
Product description	512 Kbit serial SPI bus EEPROM with high-speed clock
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	subcon Amkor, Philippines	subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	subcon Amkor, Philippines	subcon Amkor, Philippines
WLCSP	subcon Stats ChipPac, Singapore	subcon Stats ChipPac, Singapore

Reliability assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the improved design M95512 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for M95512-W devices
- 1.8 to 5.5 V at –40 to 85 °C for M95512-R devices
- 1.7 to 5.5 V at –40 to 85 °C for M95512-DF devices

The CMOSF8H is a new advanced silicon process technology that has already been qualified in the STMicroelectronics Rousset 8” diffusion plant, and is in production for M24M02/M95M02, M24M01/M95M01, M24512/M95512, M24256/M95256, M24C64/M95640 and M24C32/M95320 EEPROM products. This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The improved design M95512 using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed all the reliability requirements.

Refer to *Section 3: Reliability test results* for details.

2 Device characteristics

Device description

The M95512 devices are electrically erasable programmable memories (EEPROMs) organized as 65536 x 8 bits, accessed through the SPI bus.

The M95512 devices can operate with a supply range from 1.7 V up to 5.5 V, and are guaranteed over the -40 °C/+85 °C temperature range.

The M95512-DF offers an additional page, named the identification page(128 bytes). The identification page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The SPI bus signals are C, D and Q. The device is selected when the Chip Select ($\overline{S}$) signal is driven low. Communications with the device can be interrupted when the $\overline{HOLD}$ signal is driven low.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicles used for the die qualification are presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95512	CMOSF8H	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicles used for package qualification are presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M95M02 (1)	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen / subcon Amkor
M24M01 (2)	CMOSF8H	ST Rousset 8”	TSSOP8	ST Shenzhen / subcon Amkor
M24512 (3)	CMOSF8H	ST Rousset 8”	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / subcon Amkor
M95M02 / M24512 (1)	CMOSF8H	ST Rousset 8”	WLCSP	subcon Stats ChipPac

1. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable.
3. Similar memory array and same design core between M95512 (512 Kbit SPI) and M24512 (512 Kbit I2C) (metal mask option for bus control) using the same silicon process technology in the same diffusion fab - Package qualification results on M24512 are applicable.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size
						M95512
						Lot 1
EDR	High temperature operating life after endurance					
	AEC-Q100-005	1 Million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	1	1008 hrs	0/80
	Data retention after endurance					
	AEC-Q100-005	1Million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	1008 hrs	0/80
LTOL	Low temperature operating life					
	JESD22-A108	–40 °C, 6 V	80	1	1008 hrs	0/80
HTSL	High temperature storage life					
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80
WEB	Program/erase endurance cycling + bake					
	Internal spec.	1 Million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	1 Million cycles / 48 hrs	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)					
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 4000 V
ESD MM	Electrostatic discharge (machine model)					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 400 V
LU	Latch-up (current injection and overvoltage stress)					
	AEC-Q100-004 JESD78A	At maximum operating temperature (150 °C)	6	1	N/A	Class II - Level A

1. See *Table 8: List of terms* for a definition of abbreviations.
2. First rejects after 10 million E/W cycles + bake.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M95M02 (2)			M95512
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1200	3	N/A	0/1200	0/1200	0/1200	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ELFR (3)	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	3	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M95M02 (2MB SPI) are applicable.
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24M01 (2)			M95512
						Lot1	Lot2	Lot3	Lot4
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	400	3	N/A	0/400	0/400	0/400	-
THB (3)	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.5 V	80	3	1008 hrs	0/80	0/80	0/80	-
TC (3)	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	3	1000 cycles	0/80	0/80	0/80	-
TMSK (3)	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	80	3	200 shocks	0/80	0/80	0/80	-
AC (3)	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	3	168 hrs	0/80	0/80	0/80	-
HTSL (3)	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	3	1008 hrs	0/80	0/80	0/80	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V	-	-	Pass >1500 V

1. See *Table 8: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24M01 (1MB I2C) are applicable.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78A: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 8. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Feb-2012	1	Initial release.

Document Revision History

Date	Rev.	Description of the Revision
Feb. 22 , 2012	1.00	First draft creation

Source Documents & Reference Documents

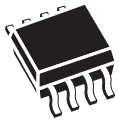
Source document Title	Rev.:	Date:

M95512-DR
M95512-R M95512-W

512 Kbit serial SPI bus EEPROM with high-speed clock

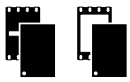
Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 512 Kb (64 Kbytes) of EEPROM
  - Page size: 128 bytes
- Additional Write lockable Page (Identification page)
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Write Protect: quarter, half or whole memory array
- High-speed clock frequency (20 MHz)
- Single supply voltage: 1.8 V to 5.5 V
- More than 1 Million Write cycles
- More than 40-year data retention
- Enhanced ESD Protection
- Packages
  - ECOPACK2® (RoHS compliant and Halogen-free)



SO8 (MN)
150 mils width

TSSOP8 (DW)
169 mils width



UFDFPN8 (MB, MC)
2 × 3 mm (MLP)

WLCSP (CS)

Contents

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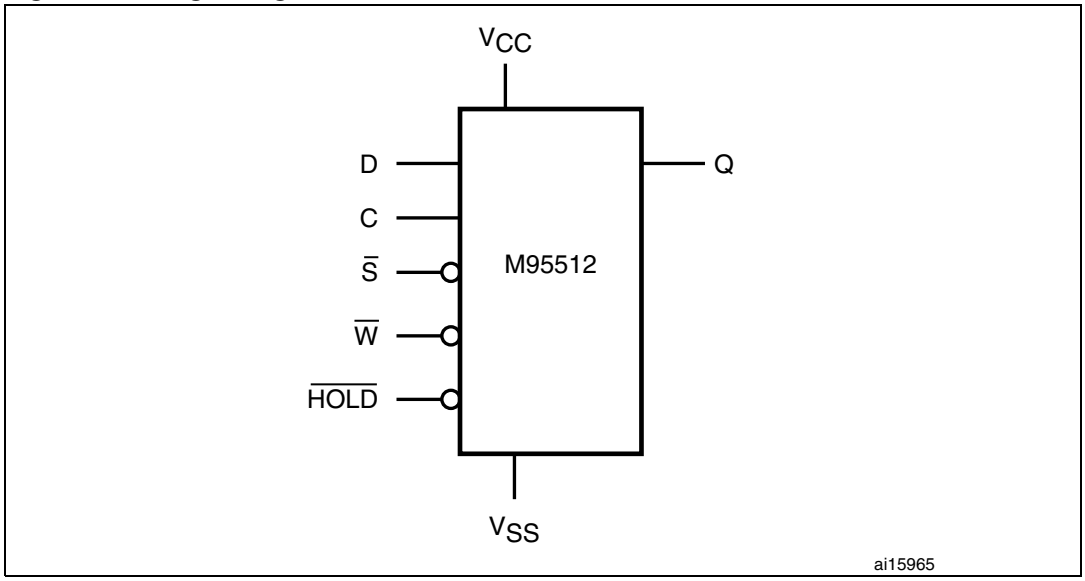
1 Description

The M95512-W, M95512-R and M95512-DR are electrically erasable programmable memory (EEPROM) devices accessed by a high-speed SPI-compatible bus. In the rest of the document these devices are referred to as M95512, unless otherwise specified.

The M95512-DR also offers an additional page, named the Identification Page (128 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as it can be used to store unique identification parameters and/or parameters specific to the production line.

Figure 1. Logic diagram



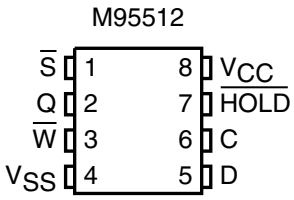
The memory array is organized as 65536 × 8 bit. The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 1* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Table 1. Signal names

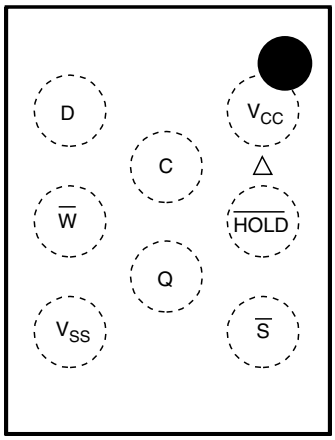
Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
S	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package (SO8, TSSOP8, UFDFPN8) connections



1. See *Section 11: Package mechanical data* for package dimensions, not and how to identify pin-1.

Figure 3. WLCSP connections (top view, marking side, with balls on the underside)



Caution: As EEPROM cells loose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 14* and *Table 16*). These signals are described next.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

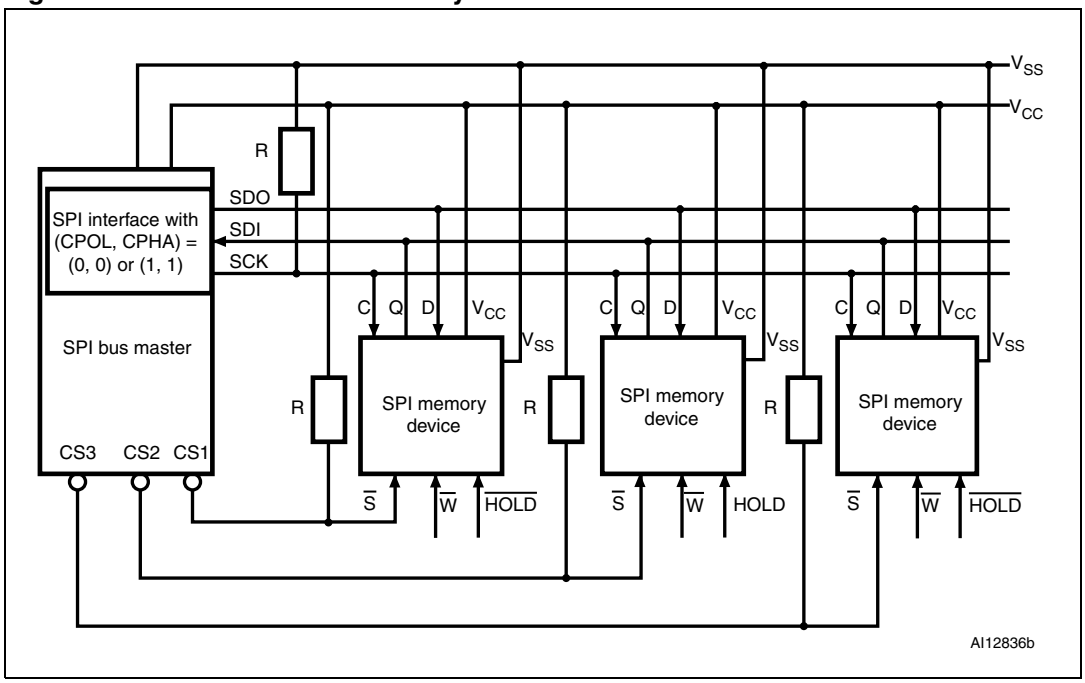
3 Connecting to the SPI bus

These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 4. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

Figure 4 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, the other devices are high impedance.

A pull-up resistor connected on each /S input (represented in *Figure 4*) ensures that each slave device on the SPI bus is not selected if the bus master leaves the /S line in the high impedance state.

In applications where the Bus Master might enter a state where all inputs/outputs SPI lines are in high impedance at the same time (for example, if the Bus Master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high). This ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met.

The typical value of R is 100 kΩ,.

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

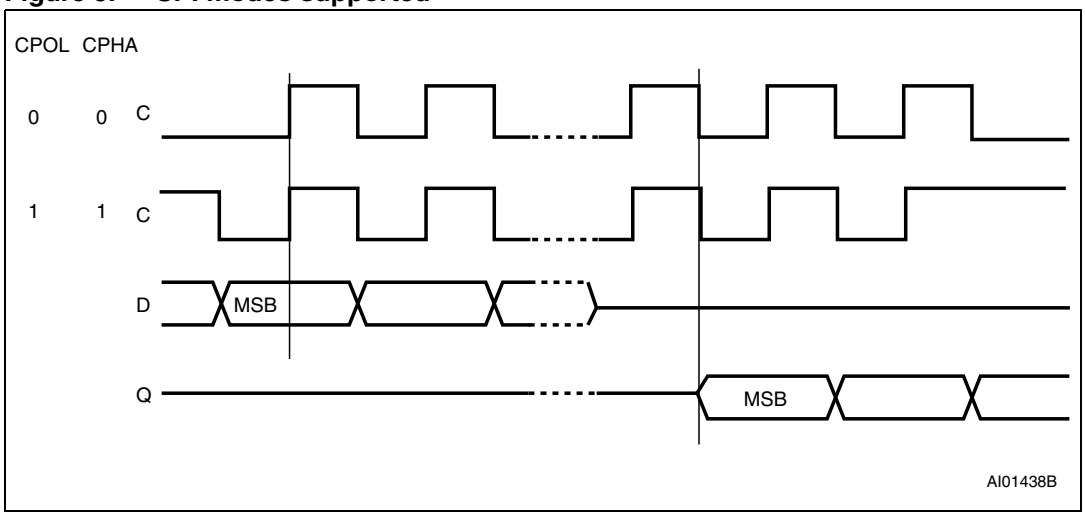
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8* and *Table 10*.). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

4.1.2 Device reset

In order to prevent inadvertent Write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} has reached the POR threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8* and *Table 10*).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the Standby Power mode
- deselected (note that when the device is deselected it is necessary to apply a falling edge on Chip Select ($\overline{S}$) prior to issuing any new instruction, otherwise the instruction is not executed)
- Status register values:
  - the Write Enable Latch (WEL) bit is reset to 0
  - the Write In Progress (WIP) bit is reset to 0
  - the SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode, however, the device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 8* and *Table 10*.

4.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 4*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8* and *Table 10* and the rise time must not vary faster than 1 V/µs.

4.1.4 Power-down

During power-down (continuous decrease in V_{CC} below the minimum V_{CC} operating voltage defined in *Table 8* and *Table 10*), the device must be:

- deselected (Chip Select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (that is there should not be any internal write cycle in progress).

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 16*.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to I_{CC1}.

4.3 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress[1][2].

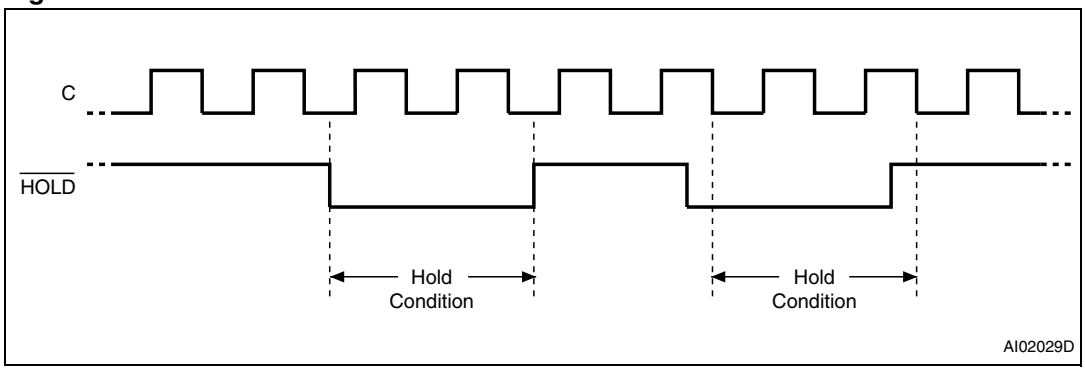
The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 6*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 6 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

1. This resets the internal logic, except the WEL and WIP bits of the Status Register.
2. In the specific case where the device has shifted in a Write command (Inst + Address + data bytes, each data byte being exactly 8 bits), deselecting the device also triggers the write cycle of this decoded command.

Figure 6. Hold condition activation



4.4 Status register

Figure 7 shows the position of the Status register in the control logic of the device. The Status register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status register bits.

Table 2. Write-protected block size

Status register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	none	none
0	1	Upper quarter	C000h - FFFFh
1	0	Upper half	8000h - FFFFh
1	1	Whole memory	0000h - FFFFh

4.5 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits in the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

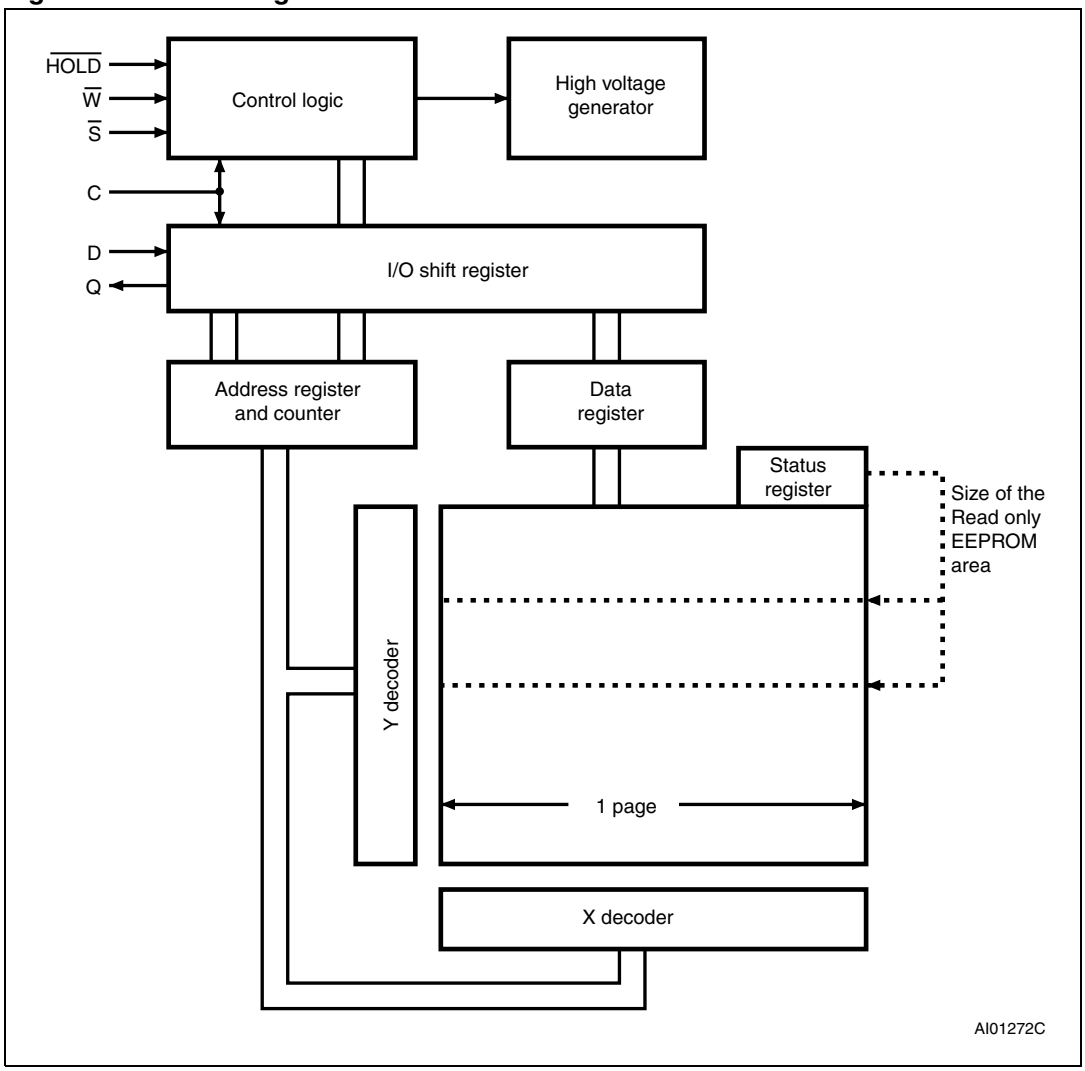
Two points need to be noted in the previous sentence:

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

5 Memory organization

The memory is organized as shown in *Figure 7*.

Figure 7. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device automatically deselects itself.

Table 3. M95512-W and M95512-R instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

Table 4. M95512-DR instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
Read Identification Page	Reads the page dedicated to identification.	1000 0011(1)
Write Identification Page	Writes the page dedicated to identification.	1000 0010(1)
Read Lock Status	Reads the lock status of the Identification Page.	1000 0011(2)
Lock ID	Locks the Identification page in read-only mode.	1000 0010(2)

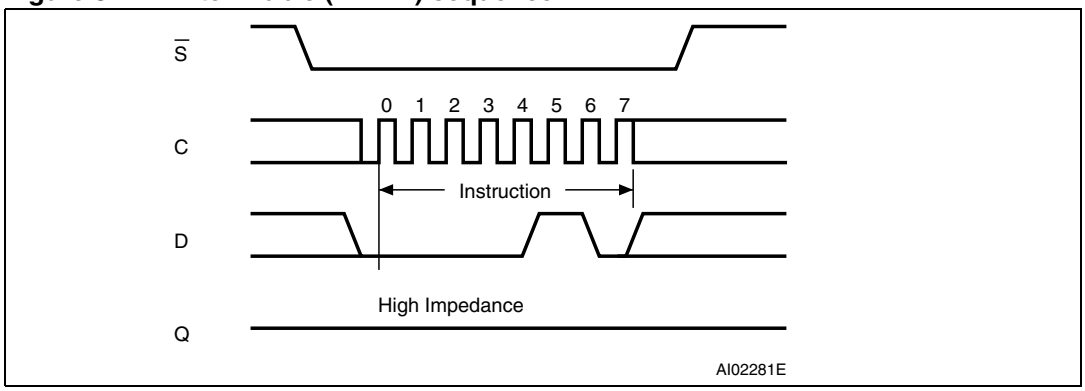
1. Address bit A10 must be 0, all other address bits are Don't Care.
2. Address bit A10 must be 1, all other address bits are Don't Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 8. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

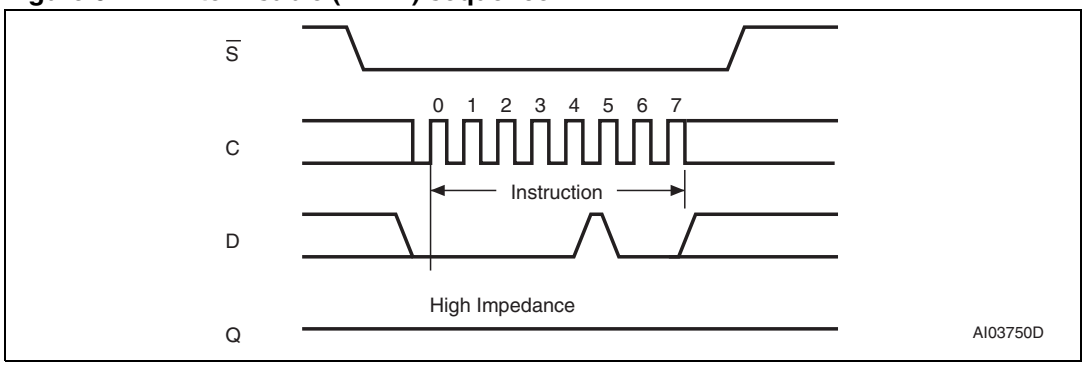
As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 9. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 5*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 5. Status register format

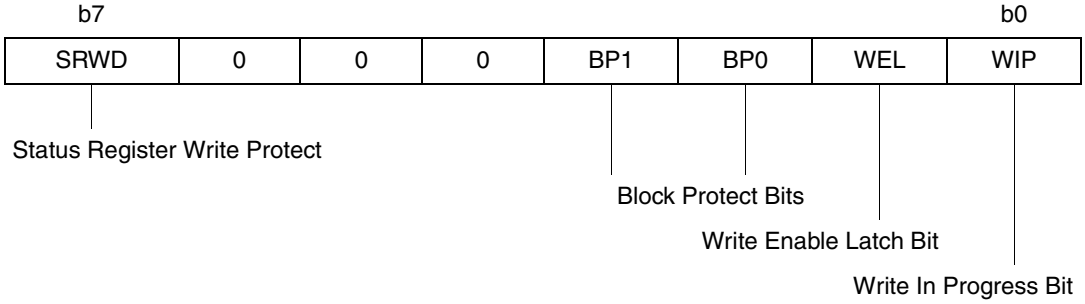
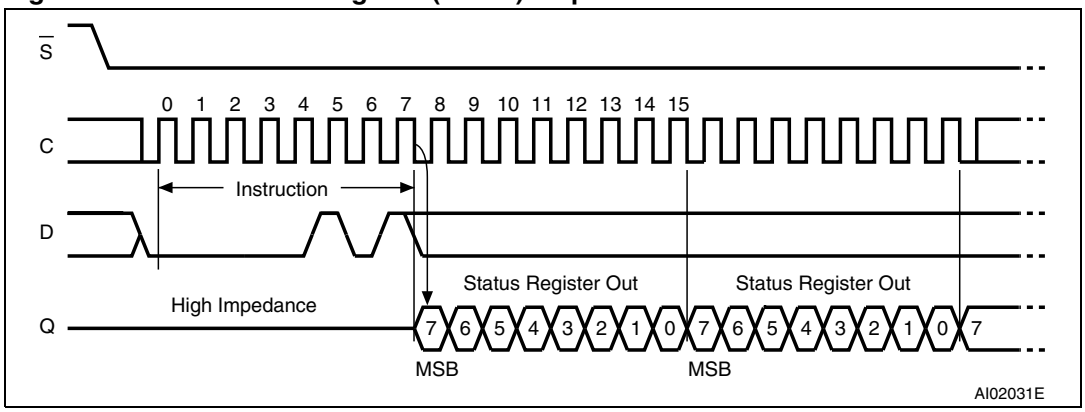


Figure 10. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before a WRSR instruction can be accepted, a Write Enable (WREN) instruction must have been executed.

The Write Status Register (WRSR) instruction is issued by driving Chip Select ($\overline{S}$) low, sending the instruction code and the data byte on Serial Data input (D) and driving Chip Select ($\overline{S}$) high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not properly executed.

Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed Write cycle whose duration is t_W (specified in *Table 17* and *Table 19*). The instruction sequence is shown in *Figure 11*.

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit: the WIP bit is 1 during the self-timed Write cycle t_W, and 0 when the Write cycle is complete. The WEL bit (Write Enable Latch) is also reset when the Write cycle t_W is complete.

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 and SRWD bits:

- The Block Protect (BP1, BP0) bits define the size of the area to be treated as read-only, as defined in *Table 6*.
- The SRWD bit (Status Register Write Disable bit), depending on the signal applied on the Write Protect pin ($\overline{W}$), allows the user to set or reset the write protection mode of the Status Register. When the Status Register is in the Write-protected mode, the Write Status Register (WRSR) instruction is *not* executed.

The contents of the SRWD and BP1, BP0 bits are updated upon completion of the WRSR instruction (after t_W).

The Write Status Register (WRSR) instruction has no effect on Status Register bits b6, b5, b4, b1, b0. They are always read as 0.

Figure 11. Write Status Register (WRSR) sequence

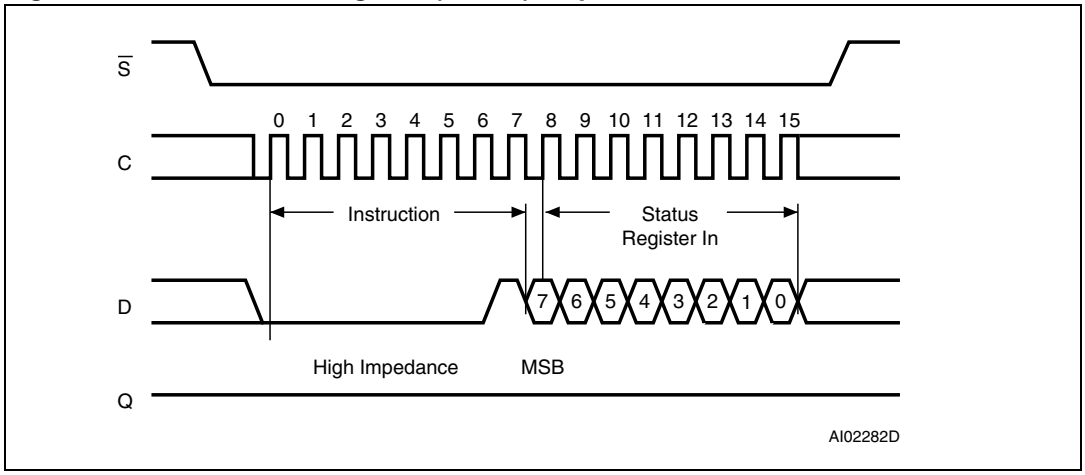


Table 6. Protection modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write Protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write Protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 2*.

The protection features of the device are summarized in *Table 6*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction), regardless of the logic level applied on the Write Protect (W) input pin.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$) input pin:

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register (provided that the WEL bit has previously been set by a WREN instruction.
- If Write Protect ($\overline{W}$) is driven low, it is not possible to write to the Status Register even if the WEL bit has previously been set by a WREN instruction (attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software-protected (SPM) by the Block Protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered either:

- by setting the SRWD bit after driving the Write Protect ($\overline{W}$) input pin low
- or by driving the Write Protect ($\overline{W}$) input pin low after setting the SRWD bit

Once entered, the Hardware-protected mode (HPM) can only be exited by pulling Write Protect ($\overline{W}$) high.

If Write Protect ($\overline{W}$) is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM) using the Block Protect (BP1, BP0) bits in the Status Register, can be used.

6.5 Read from Memory Array (READ)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

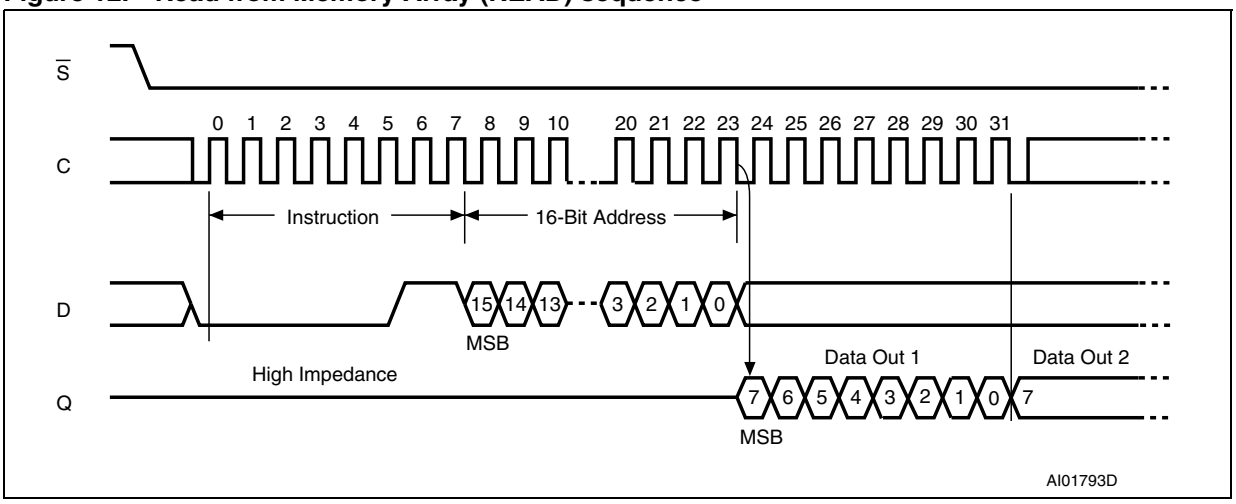
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 12. Read from Memory Array (READ) sequence



6.6 Write to Memory Array (WRITE)

As shown in *Figure 13*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle triggered by the rising edge of Chip Select ($\overline{S}$) continues for a period t_W (as specified in *Table 17* and *Table 19*), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of *Figure 13*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 14*., the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 128 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 13. Byte Write (WRITE) sequence

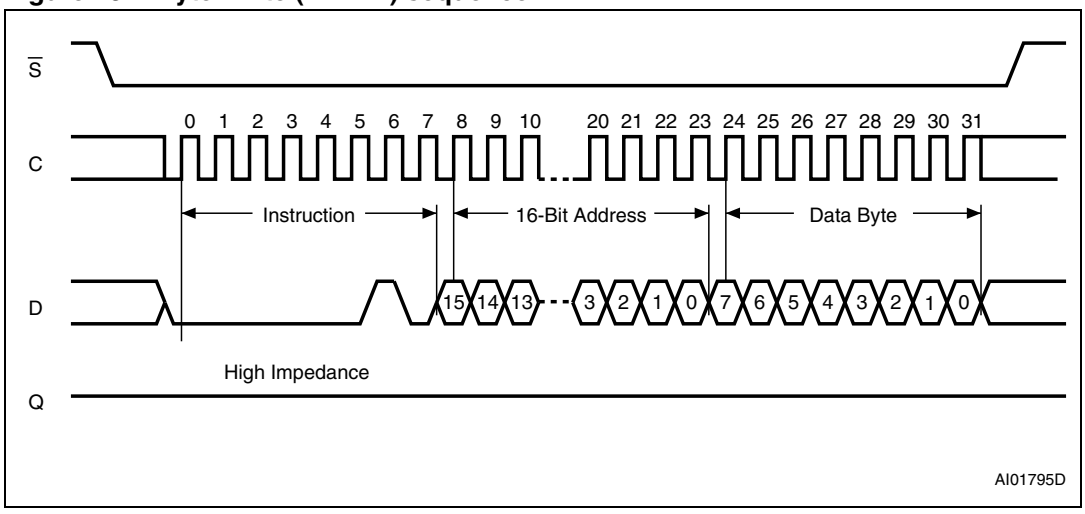
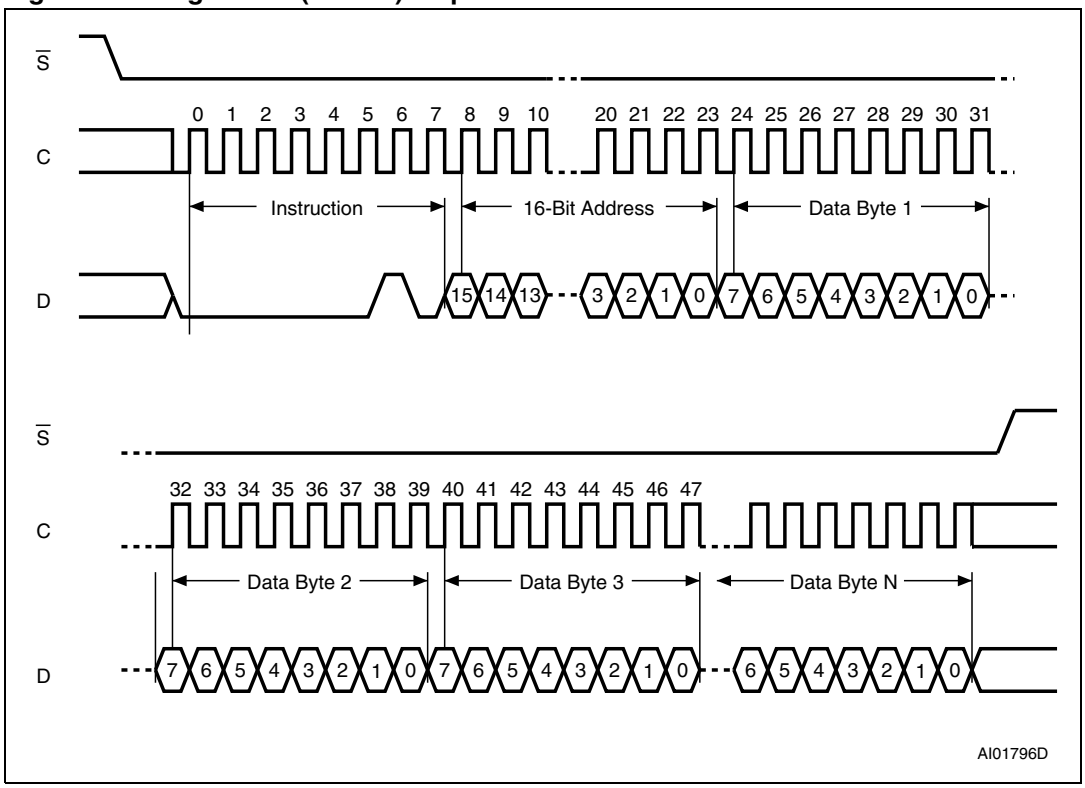


Figure 14. Page Write (WRITE) sequence



6.7 Read Identification Page (available only in M95512-DR devices)

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

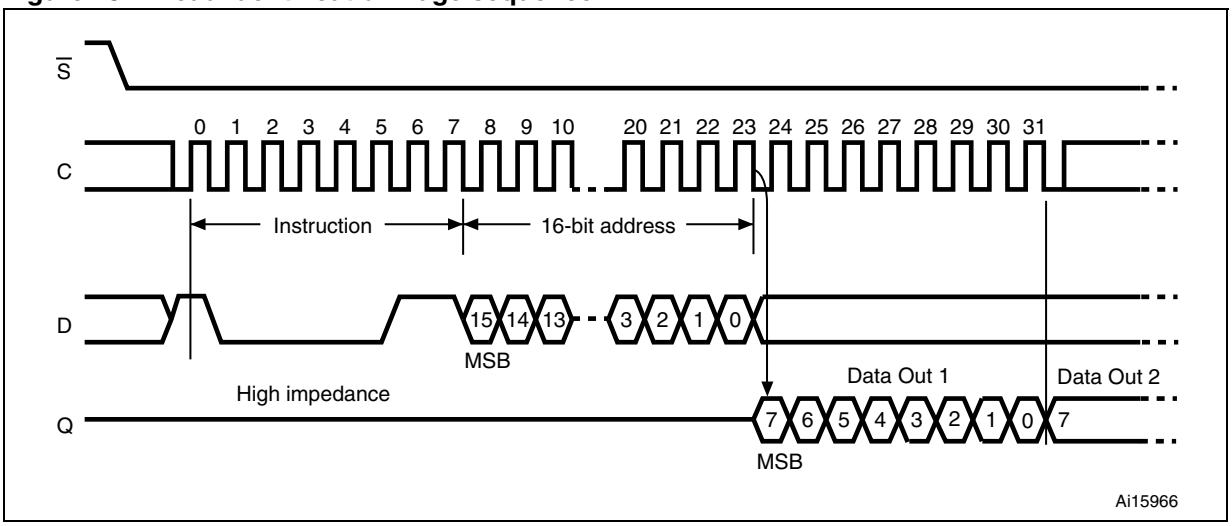
Reading this page is achieved with the Read Identification Page instruction (see *Table 4*). The Chip Select signal (S) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data input (D). Address bit A10 must be 0, address bits [A15:A11] and [A9:A7] are Don't Care, and the data byte pointed to by [A6:A0] is shifted out on Serial Data output (Q).

If Chip Select (S) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the ID page from location 90d, the number of bytes should be less than or equal to 38d, as the ID page boundary is 128 bytes).

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 15. Read Identification Page sequence



6.8 Write Identification Page (available only in M95512-DR devices)

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Writing this page is achieved with the Write Identification Page instruction (see *Table 4*), the Chip Select signal (S) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data input (D). Address bit A10 must be 0, address bits [A15:A11] and [A9:A7] are Don't Care, the [A6:A0] address bits define the byte address inside the identification page.

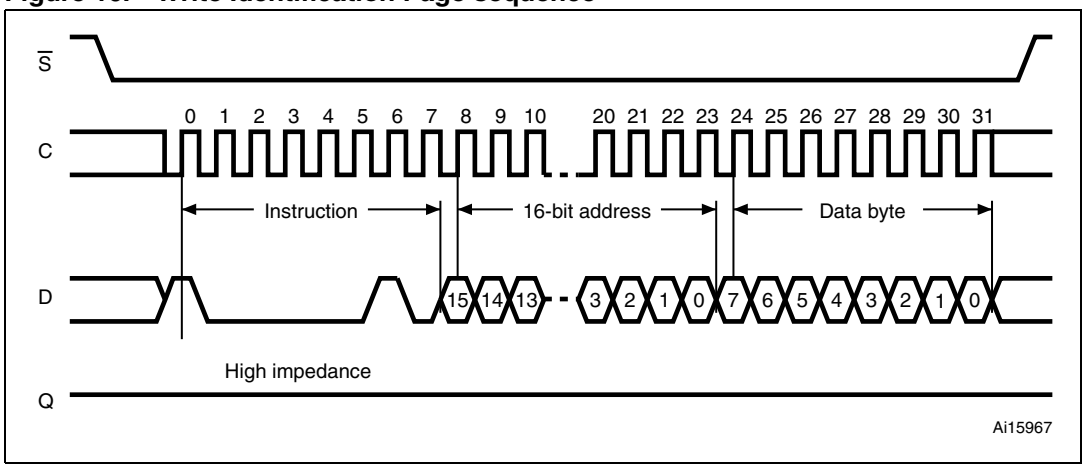
The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed write cycle triggered by the rising edge of Chip Select ($\overline{S}$) continues for a period t_W (as specified in *Table 18* and *Table 19*), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of *Figure 16*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 16*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 128 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction)
- if Status register bits (BP1, BP0) = (1, 1)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in)
- if the Identification page is locked by the Lock Status bit

Figure 16. Write Identification Page sequence



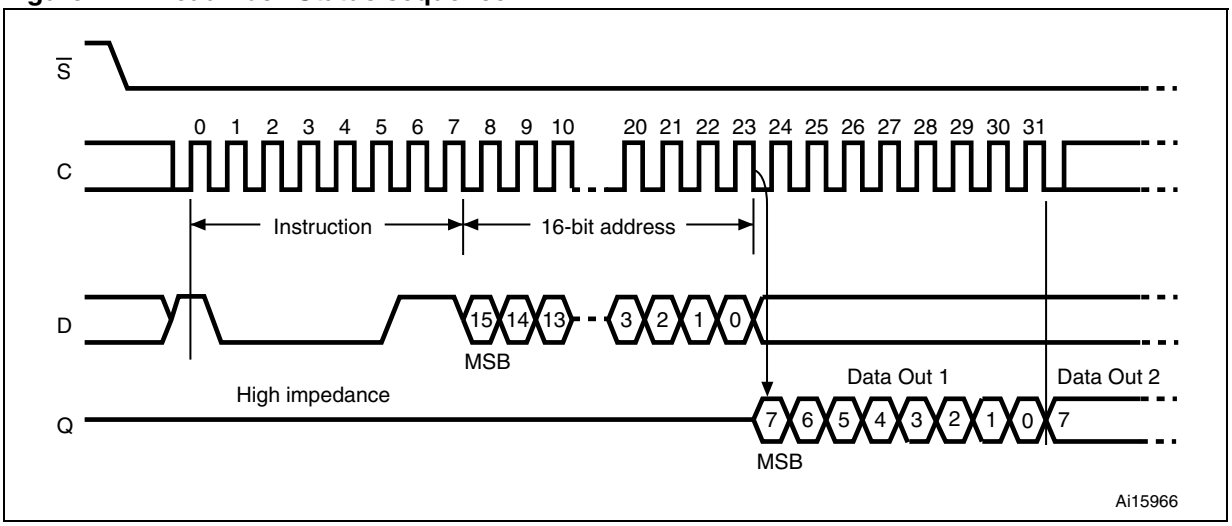
6.9 Read Lock Status (available only in M95512-DR devices)

The Read Lock Status instruction (see *Table 4*) allows to check if the Identification Page is locked (or not) in read-only mode. The Read Lock Status sequence is defined with the Chip Select (S) first driven low. The bits of the instruction byte and address bytes are then shifted in on Serial Data input (D). Address bit A10 must be 1, all other address bits are Don't Care.

The Lock bit is the LSB (least significant bit) of the byte read on Serial Data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving Chip Select ($\overline{S}$) high.

The instruction sequence is shown in *Figure 17*.

Figure 17. Read Lock Status sequence



6.10 Lock ID (available only in M95512-DR devices)

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. The Lock ID instruction is issued by driving Chip Select ($\overline{S}$) low, sending the instruction code, the address and a data byte on Serial Data input (D), and driving Chip Select ($\overline{S}$) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

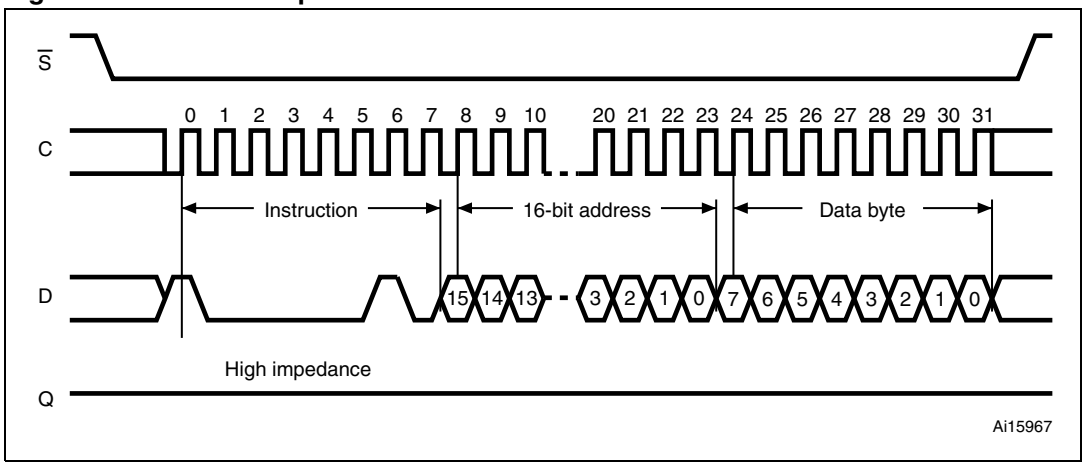
Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Lock ID instruction is not executed.

Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is t_W (specified in *Table 18* and *Table 19*). The instruction sequence is shown in *Figure 18*.

The instruction is not accepted, and so not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction)
- if Status register bits (BP1,BP0) = (1,1)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in)
- if the Identification page is locked by the Lock Status bit

Figure 18. Lock ID sequence



7 ECC (error correction code) and write cycling

The M95512-W, M95512-R and M95512-DR devices offer an ECC (error correction code) logic which compares each 4-byte word with its associated 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the other three bytes making up the word. It is therefore recommended to write data by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

The M95512-W, M95512-R and M95512-DR devices are qualified at 1 million (1 000 000) Write cycles, using a cycling routine that writes to the device by multiples of 4-byte packets.

8 Power-up and delivery state

8.1 Power-up state

After power-up, the device is in the following state:

- Standby Power mode
- Deselected (after Power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- Not in the Hold Condition
- Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

8.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

9 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient temperature with power applied	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	–5	-	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–3000	+3000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100pF, R1=1500 Ω, R2=500 Ω)

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M95512-W device grade 6)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C

Table 9. Operating conditions (M95512-W device grade 3)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	125	°C

Table 10. Operating conditions (M95512-R and M95512-DR)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input Rise and Fall times		50	ns
	Input Pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 19. AC measurement I/O waveform

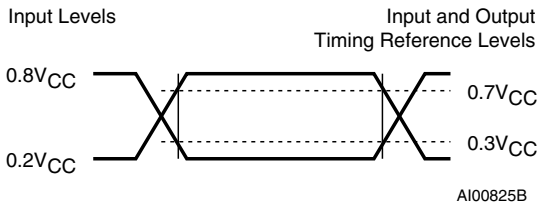


Table 12. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Not 100% tested.

Table 13. Memory cell characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
N_{cycle}	Endurance	TA = 25°C, 1.8V < Vcc < 5.5V	1,000,000	-	Write cycle

Note: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please refer to AN2014.

Table 14. DC characteristics (current(1) M95512-W products)

Symbol	Parameter	Test conditions: V_{CC} = 2.5 to 5.5 V at T_A = –40 to 85 °C (device grade 6) or T_A = –40 to 125 °C (device grade 3)	Min.	Max.	Unit
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		3	mA
		C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		5	mA
I_{CC0}(2)	Supply current (Write)	During t_W, $\overline{S}$ = V_{CC}, 2.5 V < V_{CC} < 5.5 V		6	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, 2.5 V < V_{CC} < 5.5 V		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V and I_{OL} = 1.5 mA or V_{CC} = 5 V and I_{OL} = 2 mA		0.4	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V and I_{OH} = –0.4 mA or V_{CC} = 5 V and I_{OH} = –2 mA	0.8 V_{CC}		V

1. Current products are identified by AB process letters AB.
2. Characterized value, not tested in production.

Table 15. DC characteristics (new[1] M95512-W products)

Symbol	Parameter	Test conditions: V_{CC} = 2.5 to 5.5 V, T_A = –40 to 85 °C	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 2.5 V, Q = open		4	mA
		C = 0.1V_{CC}/0.9V_{CC} at 20 MHz, V_{CC} = 5 V, Q = open		8	mA
I_{CC0}[2]	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$, 2.5 V < V_{CC} < 5.5 V		6	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 2.5 V < V_{CC} < 5.5 V		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V and I_{OL} = 1.5 mA or V_{CC} = 5 V and I_{OL} = 2 mA		0.4	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V and I_{OH} = –0.4 mA or V_{CC} = 5 V and I_{OH} = –2 mA	0.8 V_{CC}		V

1. New products are identified by process letter K.
2. Characterized value, not tested in production.

Table 16. DC characteristics (current and new M95512-R and M95512-DR products)[1]

Symbol	Parameter	Test conditions: V_{CC} = 1.8 to 5.5 V, T_A = –40 to 85 °C	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1V_{CC}/0.9V_{CC} at 2 MHz, V_{CC} = 1.8 V, Q = open[2]		1	mA
		C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 1.8 V, Q = open[3]		2.5	mA
I_{CC0}[4]	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$, 1.8 V < V_{CC} < 2.5 V		3	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 1.8 V < V_{CC} < 2.5 V		3	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

1. If the application uses the M95512-R or M95512-DR with 2.5 V < VCC < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 13* and *Table 14* instead of the above table.
2. Current products are identified by process letters AB.
3. New products are identified by process letter K.
4. Characterized value, not tested in production.

Table 17. AC characteristics (current[1] M95512-W products)

Test conditions: V_{CC} = 2.5 to 5.5 V at T_A = –40 to 85 °C (device grade 6) or T_A = –40 to 125 °C (device grade 3)					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		ns
t_{CH} (2)	t_{CLH}	Clock high time	90		ns
t_{CL} (2)	t_{CLL}	Clock low time	90		ns
t_{CLCH} (3)	t_{RC}	Clock rise time		1	µs
t_{CHCL} (3)	t_{FC}	Clock fall time		1	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	30		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ} (3)	t_{DIS}	Output disable time		100	ns
t_{CLQV}	t_V	Clock low to output valid		60	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH} (3)	t_{RO}	Output rise time		50	ns
t_{QHQL} (3)	t_{FO}	Output fall time		50	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50	ns
t_{HLQZ} (3)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		100	ns
t_W	t_{WC}	Write time		5	ms

1. Current products are identified by process letters AB.
2. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
3. Value guaranteed by characterization, not 100% tested in production.

Table 18. AC characteristics (New(1) M95512-W products)

Test conditions: V_{CC} = 2.5 to 5.5 V, T_A = –40 to 85 °C							
Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Unit
			2.5 V to 5.5 V		4.5 V to 5.5 V		
f_C	f_{SCK}	Clock frequency	D.C.	10	D.C.	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		15		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		15		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		20		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		15		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		15		ns
t_{CH} (2)	t_{CLH}	Clock high time	45		20		ns
t_{CL} (2)	t_{CLL}	Clock low time	45		20		ns
t_{CLCH} (3)	t_{RC}	Clock rise time		2		2	µs
t_{CHCL} (3)	t_{FC}	Clock fall time		2		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		5		ns
t_{CHDX}	t_{DH}	Data in hold time	10		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		15		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		15		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		0		ns
t_{SHQZ} (3)	t_{DIS}	Output disable time		40		20	ns
t_{CLQV}	t_V	Clock low to output valid		40		20	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
t_{QLQH} (3)	t_{RO}	Output rise time		40		20	ns
t_{QHQL} (3)	t_{FO}	Output fall time		40		20	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40		20	ns
t_{HLQZ} (3)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		40		20	ns
t_W	t_{WC}	Write time		5		5	ms

1. New products are identified by process letter K.
2. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
3. Value guaranteed by characterization, not 100% tested in production.

Table 19. AC characteristics (current and new M95512-R and M95512-DR products)(1)

Test conditions: V_{CC} = 1.8 to 5.5 V, T_A = –40 to 85 °C							
Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Unit
			Current(2) products		New products(3)		
f_C	f_{SCK}	Clock frequency	D.C.	2	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	200		60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	200		60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	200		90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	200		60		ns
t_{CHSL}		$\overline{S}$ not active hold time	200		60		ns
t_{CH} (4)	t_{CLH}	Clock high time	200		80		ns
t_{CL} (4)	t_{CLL}	Clock low time	200		80		ns
t_{CLCH} (5)	t_{RC}	Clock rise time		1		2	µs
t_{CHCL} (5)	t_{FC}	Clock fall time		1		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	40		20		ns
t_{CHDX}	t_{DH}	Data in hold time	50		20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	140		60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	90		60		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		0		ns
t_{SHQZ} (5)	t_{DIS}	Output disable time		250		80	ns
t_{CLQV}	t_V	Clock low to output valid		150		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
t_{QLQH} (5)	t_{RO}	Output rise time		100		80	ns
t_{QHQL} (5)	t_{FO}	Output fall time		100		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		100		80	ns
t_{HLQZ} (5)	t_{HZ}	$\overline{HOLD}$ low to output High-Z		250		80	ns
t_W	t_{WC}	Write time		5		5	ms

1. The test flow guarantees the AC parameter values defined in this table (when V_{CC} = 1.8 V) and the AC parameter values defined in *Table 17* and *Table 18* (when V_{CC} > 2.5 V).
2. Current products are identified by process letters “AB”.
3. New products are identified by process letter K.
4. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, 1 / f_C(max)
5. Value guaranteed by characterization, not 100% tested in production.

Figure 20. Serial input timing

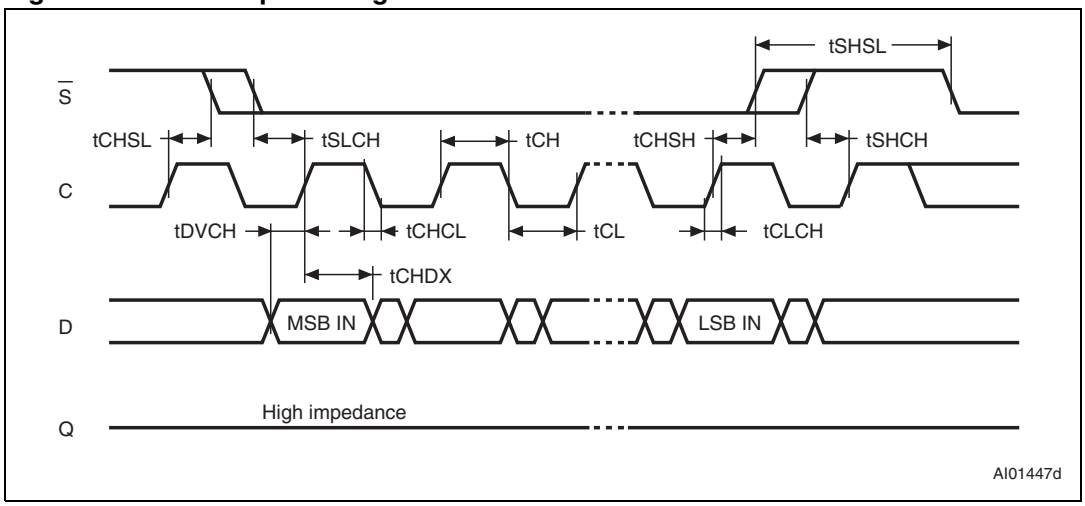


Figure 21. Hold timing

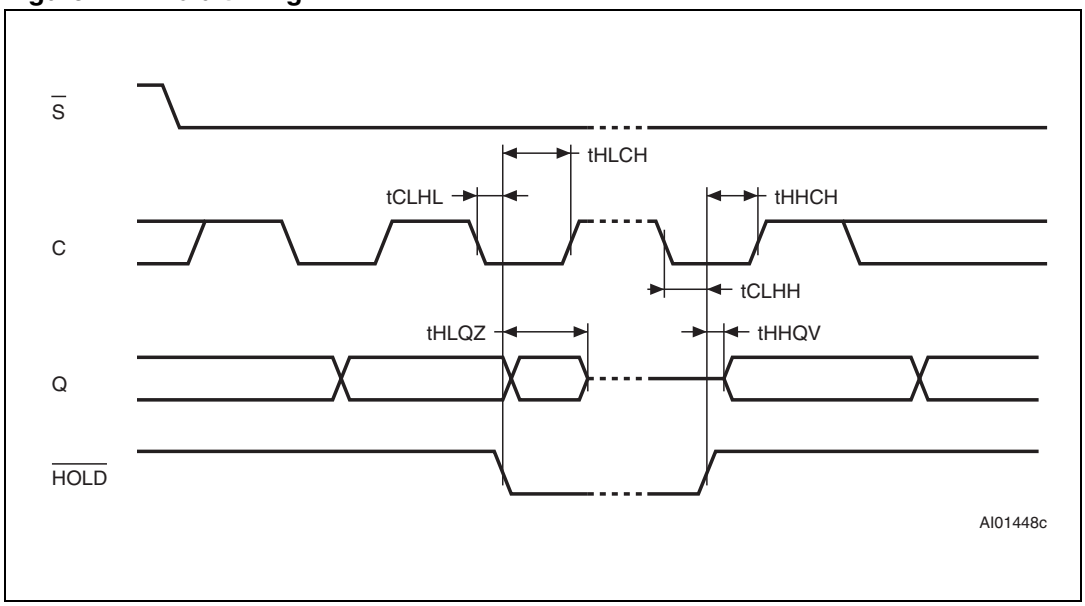
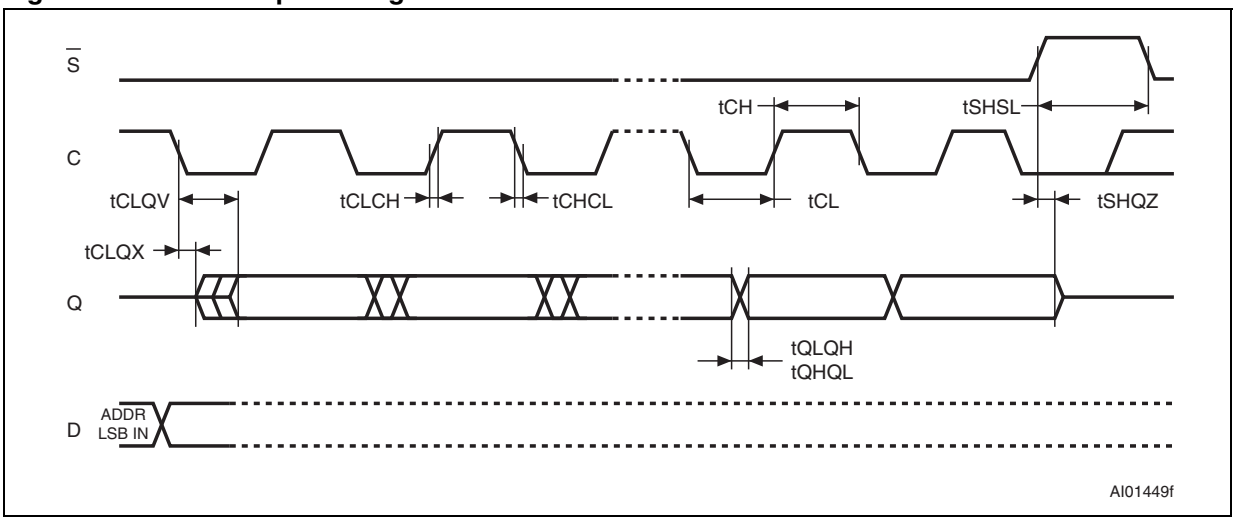


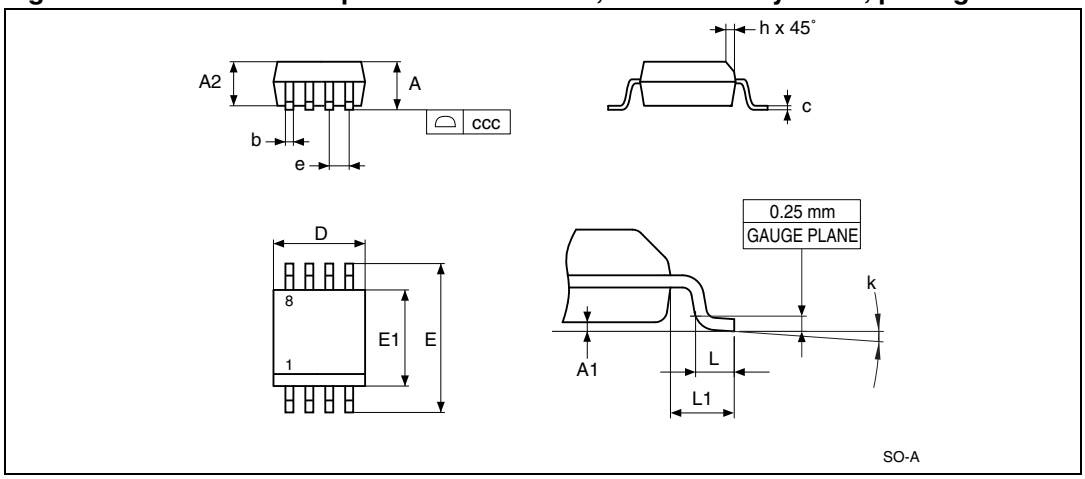
Figure 22. Serial output timing



11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 23. SO8N – 8 lead plastic small outline, 150 mils body width, package outline



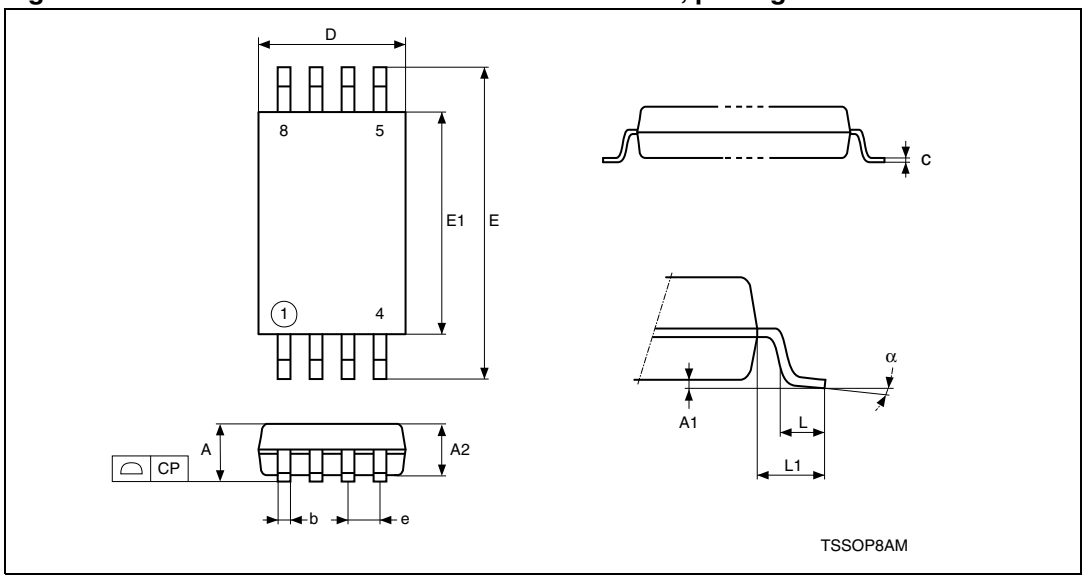
1. Drawing is not to scale.

Table 20. SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.10	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.10			0.0039
D	4.90	4.80	5.00	0.1929	0.189	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	–	–	0.05	-	-
h		0.25	0.50		0.0098	0.0197
k		0°	8°		0°	8°
L		0.40	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. TSSOP8 – 8 lead thin shrink small outline, package outline



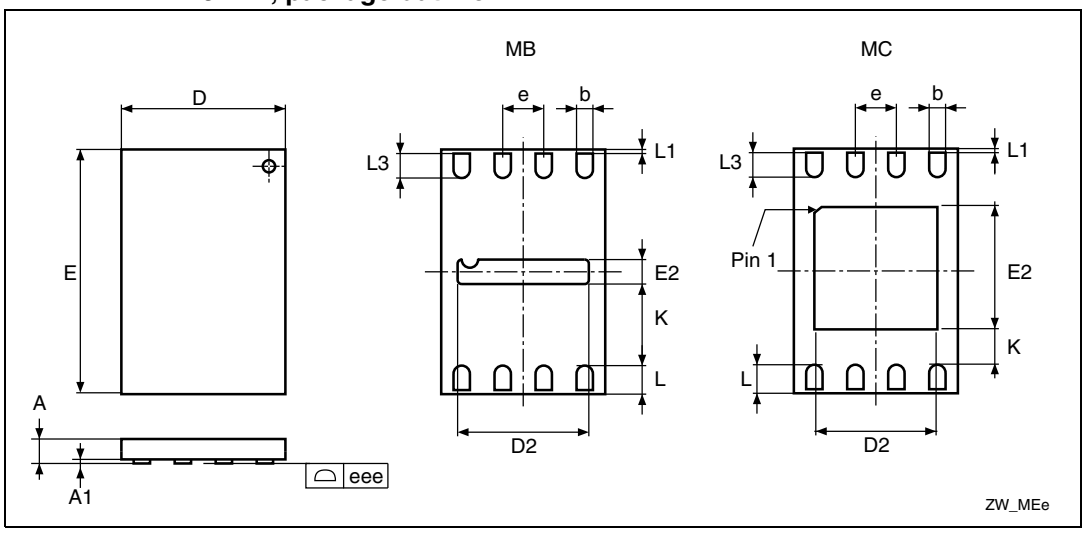
1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to VSS. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 21. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°
N	8			8		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3 mm, package outline



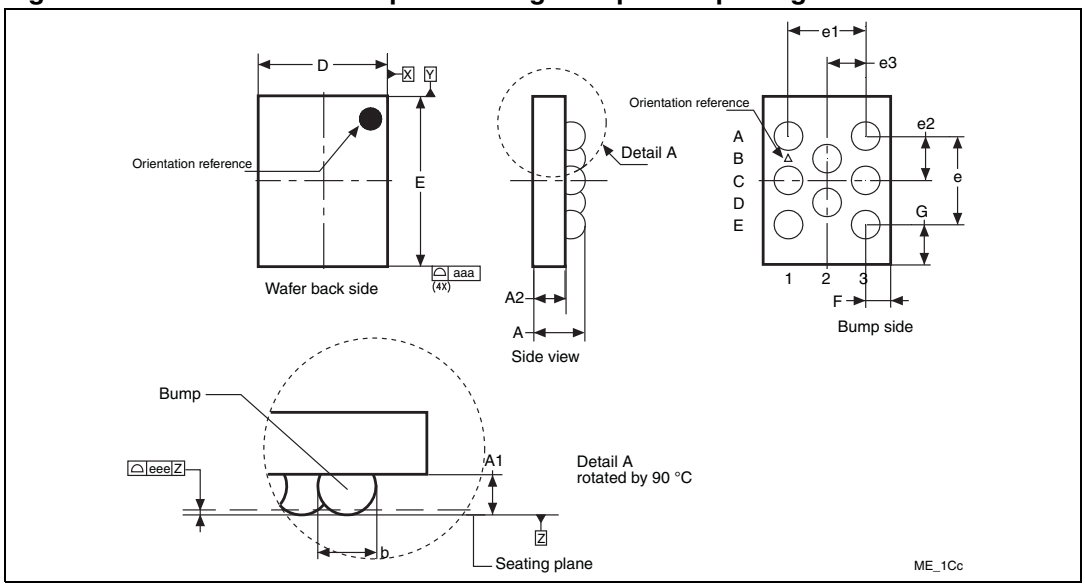
1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to VSS. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 22. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]			Note
	Typ	Min	Max	Typ	Min	Max	
A	0.550	0.450	0.600	0.0217	0.0177	0.0236	
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020	
b	0.250	0.200	0.300	0.0098	0.0079	0.0118	
D	2.000	1.900	2.100	0.0787	0.0748	0.0827	
D2 (MB)	1.600	1.500	1.700	0.0630	0.0591	0.0669	
D2 (MC)	-	1.200	1.600	-	0.0472	0.0630	
E	3.000	2.900	3.100	0.1181	0.1142	0.1220	
E2 (MB)	0.200	0.100	0.300	0.0079	0.0039	0.0118	
E2 (MC)	-	1.200	1.600	-	0.0472	0.0630	
e	0.500	-	-	0.0197	-	-	
K	-	0.300	-	-	0.0118	-	
L	-	0.300	0.500	-	0.0118	0.0197	
L1	-		0.150	-	-	0.0059	
L3	-	0.300	-	-	0.0118	-	
eee[2]	0.080			0.0031			

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Excludes embedding part of exposed die paddle from measuring.

Figure 26. WLCSP-R – 8-bump wafer-length chip-scale package outline



1. Drawing is not to scale.

Table 23. WLCSP-R – 8-bump wafer-length chip-scale package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.580	0.490	0.670	0.0228	0.0193	0.0264
A1	0.230			0.0091		
A2	0.350			0.0138		
b[2]	0.322			0.0127		
D	1.433		1.548	0.0564		0.0609
E	1.901		2.016	0.0748		0.0794
e	1.000			0.0394		
e1	0.866			0.0341		
e2	0.500			0.0197		
e3	0.433			0.0170		
F	0.284			0.0112		
G	0.453			0.0178		
N (number of terminals)	8			8		
aaa	0.110			0.0043		
eee	0.060			0.0024		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Measured at the maximum bump diameter parallel to primary datum Z.

12 Part numbering

Table 24. Ordering information scheme

Example: M95512 – W MN 6 T P /AB

Device type

M95 = SPI serial access EEPROM

Device function

512 = 512 Kbit (65536 × 8)

512-D = 512 Kbit (65536 × 8) plus Identification page

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

R = V_{CC} = 1.8 V to 5.5 V

Package

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MB or MC = UFDFPN8 (MLP8)

CS = WLCSP

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

3 = Device tested with high reliability certified flow(1).
Automotive temperature range (–40 to 125 °C)

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(2)

/AB = F8L

/K = F8H

1. ST strongly recommends the use of the automotive grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. The process letters only appear in the product ordering codes of device grade 3 devices. For other devices, it is only given here as an indication of how to differentiate current from new products. To identify current from new devices, please contact your nearest ST sales office.

13 Revision history

Table 25. Document revision history

Date	Revision	Changes
Jan-1999	1.0	Document written
13-Feb-2002	2.0	Document reformatted using the new template Voltage range -S added, and -R removed Instruction Sequence illustrations updated Announcement made of planned upgrade to 10 MHz clock for the 5V, –40 to 85°C, range
05-Dec-2003	3.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V. Voltage range -R added, and -S removed
02-Apr-2004	4.0	Old versions of document completely replaced by one rewritten from M95256
03-Jan-2005	5.0	AC and DC characteristics tables updated with the performance data of the new device identified with the process letter “A”. Table 1., Product List added. AEC-Q100-002 compliance. Device Grade information clarified. t_{HHQX}, t_{CHHL} and t_{CHHH} corrected to t_{HHQV}, t_{CLHL} and t_{CLHH}, respectively. M95512 part number with 4.5V to 5.5V operating voltage range removed (related tables removed). Document status changed to Preliminary Data.
30-Jun-2005	6.0	Updated *Figure 4: Bus master and memory devices on the SPI bus* and *Figure 21: Hold timing*. *Power On Reset* information clarified. Protected Array Addresses modified in *Table 2: Write-protected block size*. Ambient Operating Temperature value added in *Table 7: Absolute maximum ratings*. Supply Current (I_{CC}) value modified for 10 MHz in *Table 14: DC characteristics (current M95512-W products)*. All values modified in *Table 19: AC characteristics (current and new M95512-R and M95512-DR products)*. Document status changed to Datasheet.

Table 25. Document revision history (continued)

Date	Revision	Changes
06-Feb-2007	7	Document reformatted. Packages are ECOPACK® compliant. 10 MHz frequency removed. *VCC supply voltage* and *VSS ground* descriptions added. *Figure 4: Bus master and memory devices on the SPI bus* modified and explanatory paragraph added. Power-up and Power On Reset paragraphs replaced by *Section 4.1: Supply voltage (VCC)*. *Section 7: ECC (error correction code) and write cycling* added. T_A max modified in *Table 8: Operating conditions (M95512-W device grade 6)*. Note modified below *Table 13: Memory cell characteristics*. C_L modified in and *Table 11: AC measurement conditions*. V_{IL} max and I_{CC0} test conditions modified in *Table 16: DC characteristics (current and new M95512-R and M95512-DR products)*. I_{CC} modified in *Table 14: DC characteristics (current M95512-W products)*, I_{CC0} added to *Table 14* and *Table 16: DC characteristics (current and new M95512-R and M95512-DR products)* modified. *Table 19: AC characteristics (current and new M95512-R and M95512-DR products)* modified. t_{SHQZ} end timing line moved back in *Figure 22: Serial output timing*. SO8N package specifications updated (see *Figure 23* and *Table 20*). Blank removed below *Plating technology* in *Table 24: Ordering information scheme*.
05-Jun-2007	8	The device endurance is specified at more than 1 000 000 (1 million) cycles (corrected on cover page).
03-Jul-2008	9	M95512-W is now available in the device grade 3 (automotive temperature range), see *Table 8 on page 32*). *Section 4.1: Supply voltage (VCC) on page 12* updated. *Section 6.4: Write Status Register (WRSR) on page 21* and *Section 6.6: Write to Memory Array (WRITE) on page 24* clarified. I_{CC0} modified in *Table 14: DC characteristics (current M95512-W products)*. *Figure 20: Serial input timing*, *Figure 21: Hold timing* and *Figure 22: Serial output timing* updated. Package mechanical data values in inches are calculated from the millimeter values and rounded to four decimal digits (see *Section 11: Package mechanical data*). *Table 25: Available M95512 products (package, voltage range, temperature grade)* added. Small text changes.
14-Apr-2009	10	M95512-DR part number added (see *Table 26: Available M95512-DR products (package, voltage range, temperature grade)*). New M95512-W, M95512-R and M95512-DR products operating at up to 20 MHz added (preliminary data). UFDFPN8 package added (see *Section 11: Package mechanical data*).

Table 25. Document revision history (continued)

Date	Revision	Changes
11-May-2009	11	V_{ESD} modified in *Table 7: Absolute maximum ratings*. Updated: – *Section 6.7: Read Identification Page (available only in M95512-DR devices)* – *Section 6.8: Write Identification Page (available only in M95512-DR devices)* – *Section 6.9: Read Lock Status (available only in M95512-DR devices)* – *Section 6.10: Lock ID (available only in M95512-DR devices)*
28-Aug-2009	12	Data related to new products are no longer preliminary. *Note 3* updated in *Table 19: AC characteristics (current and new M95512-R and M95512-DR products)*.
14-Sep-2010	13	WLCSP package added. M95512-DR added. Updated: – *Section 1: Description* – *Section 6.7: Read Identification Page (available only in M95512-DR devices)* – *Section 6.8: Write Identification Page (available only in M95512-DR devices)* – *Section 6.9: Read Lock Status (available only in M95512-DR devices)*, *Table 7: Absolute maximum ratings* Inserted Caution under *Table 1: Signal names* Added Note under *Figure 24: TSSOP8 – 8 lead thin shrink small outline, package outline*
01-Apr-2011	14	Added: – *Table 13: Memory cell characteristics*. – Note (1) under *Table 16: DC characteristics (current and new M95512-R and M95512-DR products)* – Notes (1) and (2) in *Section 4.3: Hold condition* – Note (1) under *Table 19: AC characteristics (current and new M95512-R and M95512-DR products)* Updated: – *Section 3: Connecting to the SPI bus* – *Section 7: ECC (error correction code) and write cycling* Moved from *Section 4.5: Data protection and protocol control* to *Section 4.4: Status register*. – *Table 2: Write-protected block size* Deleted: – *Table 25: Available M95512 products (package, voltage range, temperature grade)* – *Table 26: Available M95512-DR products (package, voltage range, temperature grade)*
19-Jul-2011		Renamed *Figure 2*. Added UFDFPN8 MC package. Updated disclaimer.

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