ZARLINK SEMICONDUCTOR™

ISSUE 6 March 1997

## Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 14.5V
- 14Vpp analog signal capability
- $R_{ON}$ 65Ω max. @ $V_{DD}$=14V, 25°C
- $\Delta R_{ON}$ ≤10Ω @ $V_{DD}$=14V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology

## Applications

- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

**Ordering Information**

| | |
|---|---|
| MT8812AE | 40 Pin Plastic DIP |
| MT8812AP | 44 Pin PLCC |

**0° to 70°C**

## Description

The Zarlink MT8812 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

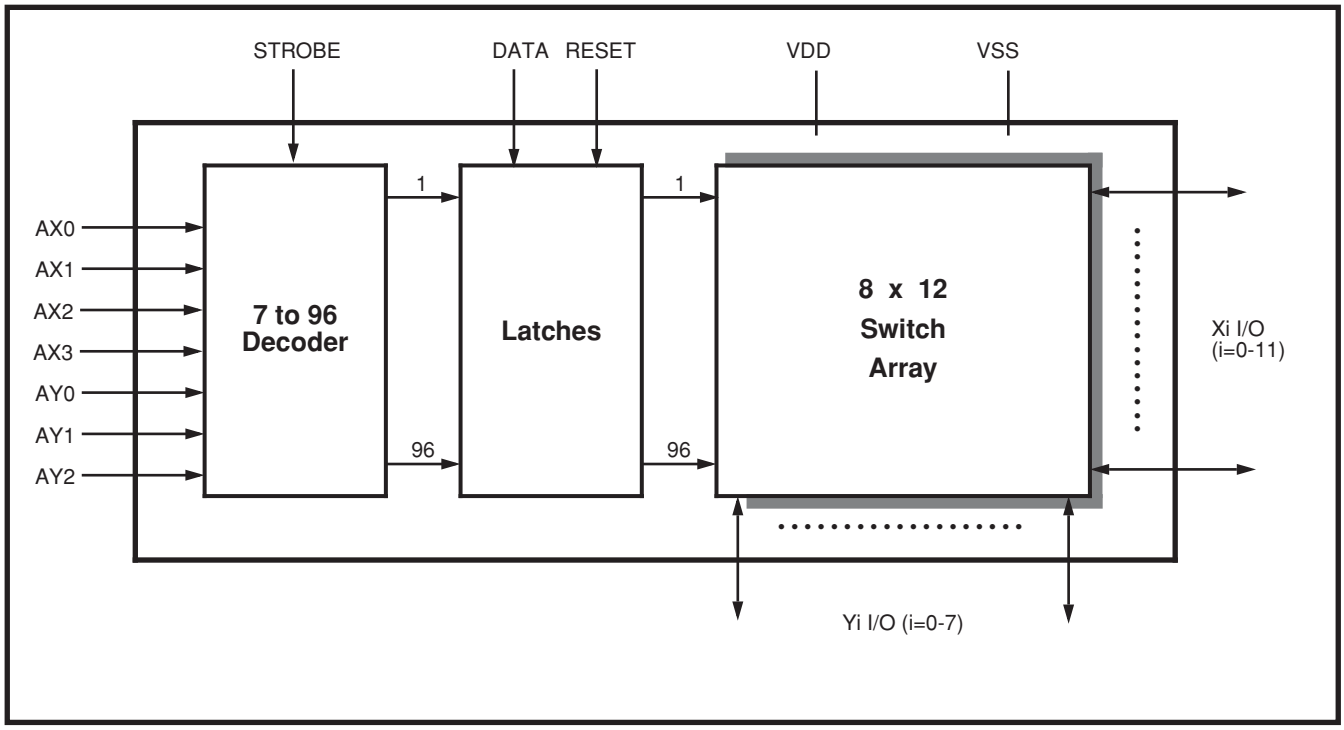



**Figure 1 - Functional Block Diagram**

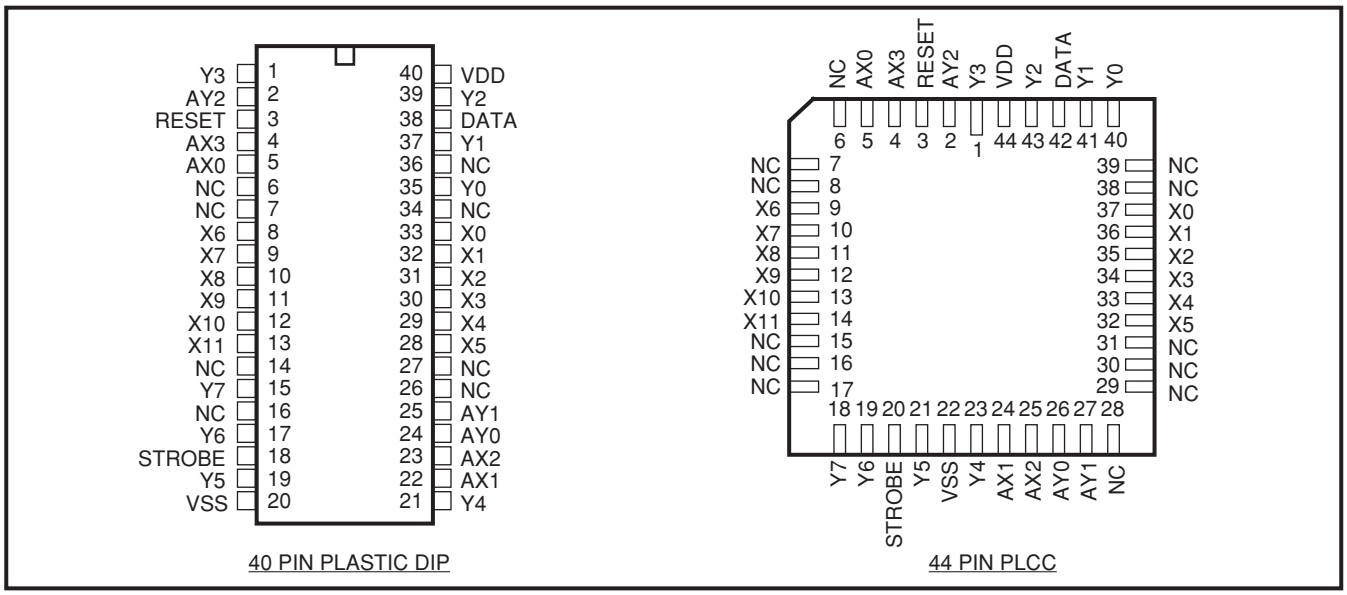



**Figure 2 - Pin Connections**

## Pin Description

| Pin # | | Name | Description |
|---|---|---|---|
| | | | |
| 1 | 1 | Y3 | **Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array. |
| 2 | 2 | AY2 | **Y2 Address Line (Input)**. |
| 3 | 3 | RESET | **Master RESET (Input):** this is used to turn off all switches. Active High. |
| 4,5 | 4,5 | AX3,AX0 | **X3 and X0 Address Lines (Inputs)**. |
| 6,7 | 6-8 | NC | **No Connection.** |
| 8-13 | 9-14 | X6-X11 | **X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array. |
| 14 | 15-17 | NC | **No Connection.** |
| 15 | 18 | Y7 | **Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array. |
| 16 | - | NC | **No Connection.** |
| 17 | 19 | Y6 | **Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array. |
| 18 | 20 | STROBE | **STROBE (Input)**: enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. |
| 19 | 21 | Y5 | **Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array. |
| 20 | 22 | $V_{SS}$ | **Ground Reference.** |
| 21 | 23 | Y4 | **Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array. |
| 22, 23 | 24,25 | AX1,AX2 | **X1 and X2 Address Lines (Inputs)**. |
| 24, 25 | 26,27 | AY0,AY1 | **Y0 and Y1 Address Lines (Inputs)**. |
| 26, 27 | 28-31 | NC | **No Connection.** |
| 28 - 33 | 32-37 | X5-X0 | **X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array. |
| 34 | 38,39 | NC | **No Connection.** |
| 35 | 40 | Y0 | **Y0 Analog (Input/Output)**: this is connected to the Y0 column of the switch array. |
| 36 | - | NC | **No Connection.** |
| 37 | 41 | Y1 | **Y1 Analog (Input/Output)**: this is connected to the Y1 column of the switch array. |
| 38 | 42 | DATA | **DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. |
| 39 | 43 | Y2 | **Y2 Analog (Input/Output)**: this is connected to the Y2 column of the switch array. |
| 40 | 44 | $V_{DD}$ | **Positive Power Supply.** |

## Functional Description

The MT8812 is an analog switch matrix with an array size of 8 x 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchro-nously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical “1” written into a memory cell turns the corresponding crosspoint switch on and a logical “0” turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical “1” on the RESET input line will asynchronously return all memory locations to logical “0” turning off all crosspoint switches.

## Address Decode

The seven address lines along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

## Absolute Maximum Ratings*

- Voltages are with respect to $V_{SS}$ unless otherwise stated.

| | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{DD}$<br>$V_{SS}$ | -0.3<br>-0.3 | 16.0<br>$V_{DD}$+0.3 | V<br>V |
| 2 | Analog Input Voltage | $V_{INA}$ | -0.3 | $V_{DD}$+0.3 | V |
| 3 | Digital Input Voltage | $V_{IN}$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| 4 | Current on any I/O Pin | I | | ±15 | mA |
| 5 | Storage Temperature | $T_S$ | -65 | +150 | °C |
| 6 | Package Power Dissipation PLASTIC DIP | $P_D$ | | 0.6 | W |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

## Recommended Operating Conditions

- Voltages are with respect to $V_{SS}$ unless otherwise stated.

| | Characteristics | Sym | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Operating Temperature | $T_O$ | 0 | 25 | 70 | °C | |
| 2 | Supply Voltage | $V_{DD}$ | 4.5 | | 14.5 | V | |
| 3 | Analog Input Voltage | $V_{INA}$ | $V_{SS}$ | | $V_{DD}$ | V | |
| 4 | Digital Input Voltage | $V_{IN}$ | $V_{SS}$ | | $V_{DD}$ | V | |

## DC Electrical Characteristics†

- Voltages are with respect to $V_{SS}$=0V, $V_{DD}$ =14V unless otherwise stated.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Quiescent Supply Current | $I_{DD}$ | | 1 | 100 | µA | All digital inputs at $V_{IN}$=$V_{SS}$ or $V_{DD}$ |
| | | | | 7 | 15 | mA | All digital inputs at $V_{IN}$=2.4V |
| 2 | Off-state Leakage Current (See G.9 in Appendix) | $I_{OFF}$ | | ±1 | ±500 | nA | $IV_{Xi} - V_{Yj}I = V_{DD} - V_{SS}$<br>See Appendix, Fig. A.1 |
| 3 | Input Logic "0" level | $V_{IL}$ | | | 0.8 | V | |
| 4 | Input Logic "1" level | $V_{IH}$ | 2.4 | | | V | |
| 5 | Input Leakage (digital pins) | $I_{LEAK}$ | | 0.1 | 10 | µA | All digital inputs at $V_{IN}$ = $V_{SS}$ or $V_{DD}$ |

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

## DC Electrical Characteristics- Switch Resistance

- $V_{DC}$ is the external DC offset applied at the analog I/O pins.

| | Characteristics | Sym | 25°C | | 60°C | | 70°C | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Typ | Max | Typ | Max | Typ | Max | | |
| 1 | On-state $V_{DD}$=14V<br>Resistance $V_{DD}$=12V<br>$V_{DD}$=10V<br>$V_{DD}$= 5V<br>(See G.1, G.2, G.3 in Appendix) | $R_{ON}$ | 45<br>60<br>65<br>145 | 65<br>85<br>95<br>220 | | | | 75<br>95<br>110<br>260 | Ω<br>Ω<br>Ω<br>Ω | $V_{SS}$=0V,$V_{DC}$=$V_{DD}$/2,<br>$IV_{Xi}$-$V_{Yj}I$ = 0.4V<br>See Appendix, Fig. A.2 |
| 2 | Difference in on-state resistance between two switches (See G.4 in Appendix) | $\Delta R_{ON}$ | 5 | 10 | | 10 | | 10 | Ω | $V_{DD}$=14V, $V_{SS}$=0,<br>$V_{DC}$=$V_{DD}$/2,<br>$IV_{Xi}$-$V_{Yj}I$ = 0.4V<br>See Appendix, Fig. A.2 |

## AC Electrical Characteristics† - Crosspoint Performance

-$V_{DC}$ is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD}$=7V, $V_{DC}$=0V, $V_{SS}$=-7V, unless otherwise stated.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Switch I/O Capacitance | $C_S$ | | 20 | | pF | f=1 MHz |
| 2 | Feedthrough Capacitance | $C_F$ | | 0.2 | | pF | f=1 MHz |
| 3 | Frequency Response Channel "ON" 20LOG($V_{OUT}/V_{Xi}$)=-3dB | $F_{3dB}$ | | 45 | | MHz | Switch is "ON"; $V_{INA}$ = 2Vpp sinewave; $R_L$ = 1kΩ See Appendix, Fig. A.3 |
| 4 | Total Harmonic Distortion (See G.5, G.6 in Appendix) | THD | | 0.01 | | % | Switch is "ON"; $V_{INA}$ = 2Vpp sinewave f= 1kHz; $R_L$=1kΩ |
| 5 | Feedthrough Channel "OFF" Feed.=20LOG ($V_{OUT}/V_{Xi}$) (See G.8 in Appendix) | FDT | | -95 | | dB | All Switches "OFF"; $V_{INA}$= 2Vpp sinewave f= 1kHz; $R_L$= 1kΩ. See Appendix, Fig. A.4 |
| 6 | Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk=20LOG ($V_{Yj}/V_{Xi}$). (See G.7 in Appendix). | $X_{talk}$ | | -45 | | dB | $V_{INA}$=2Vpp sinewave f= 10MHz; $R_L$ = 75Ω. |
| | | | | -90 | | dB | $V_{INA}$=2Vpp sinewave f= 10kHz; $R_L$ = 600Ω. |
| | | | | -85 | | dB | $V_{INA}$=2Vpp sinewave f= 10kHz; $R_L$ = 1kΩ. |
| | | | | -80 | | dB | $V_{INA}$=2Vpp sinewave f= 1kHz; $R_L$ = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit. |
| 7 | Propagation delay through switch | $t_{PS}$ | | | 30 | ns | $R_L$=1kΩ; $C_L$=50pF |

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

## AC Electrical Characteristics† - Control and I/O Timings

- $V_{DC}$ is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD}$=7V, $V_{DC}$=0V, $V_{SS}$=-7V, unless otherwise stated.

| | Characteristics | Sym | Min | Typ‡ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Control Input crosstalk to switch (for CS, DATA, STROBE, Address) | $CX_{talk}$ | | 30 | | mVpp | $V_{IN}$=3V+$V_{DC}$ squarewave; $R_{IN}$=1kΩ, $R_L$=10kΩ. See Appendix, Fig. A.6 |
| 2 | Digital Input Capacitance | $C_{DI}$ | | 10 | | pF | f=1MHz |
| 3 | Switching Frequency | $F_O$ | | | 20 | MHz | |
| 4 | Setup Time DATA to STROBE | $t_{DS}$ | 10 | | | ns | $R_L$= 1kΩ, $C_L$=50pF ①) |
| 5 | Hold Time DATA to STROBE | $t_{DH}$ | 10 | | | ns | $R_L$= 1kΩ, $C_L$=50pF ①) |
| 6 | Setup Time Address to STROBE | $t_{AS}$ | 10 | | | ns | $R_L$= 1kΩ, $C_L$=50pF )① |
| 7 | Hold Time Address to STROBE | $t_{AH}$ | 10 | | | ns | $R_L$= 1kΩ, $C_L$=50pF )① |
| 8 | STROBE Pulse Width | $t_{SPW}$ | 20 | | | ns | $R_L$= 1kΩ, $C_L$=50pF )① |
| 9 | RESET Pulse Width | $t_{RPW}$ | 40 | | | ns | $R_L$= 1kΩ, $C_L$=50pF ①) |
| 10 | STROBE to Switch Status Delay | $t_S$ | | 40 | 100 | ns | $R_L$= 1kΩ, $C_L$=50pF ①) |
| 11 | DATA to Switch Status Delay | $t_D$ | | 50 | 100 | ns | $R_L$= 1kΩ, $C_L$=50pF )① |
| 12 | RESET to Switch Status Delay | $t_R$ | | 35 | 100 | ns | $R_L$= 1kΩ, $C_L$=50pF )① |

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
)①Refer to Appendix, Fig. A.7 for test circuit.

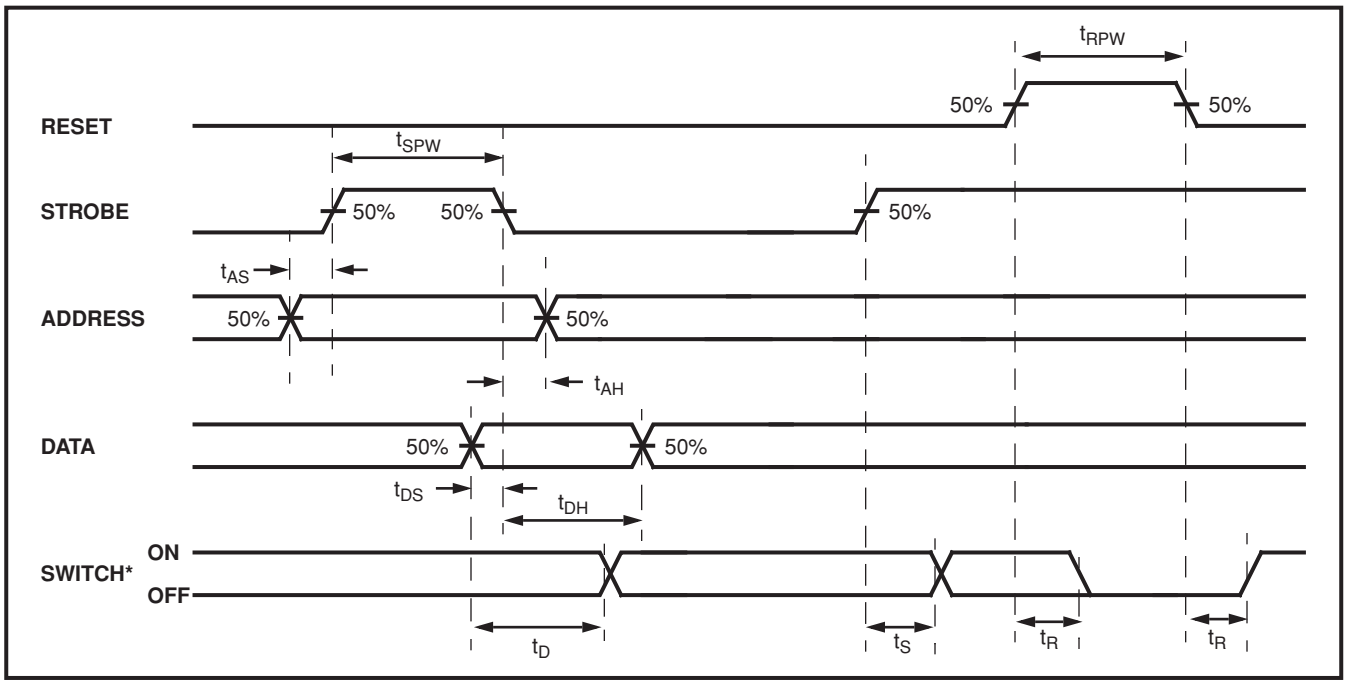


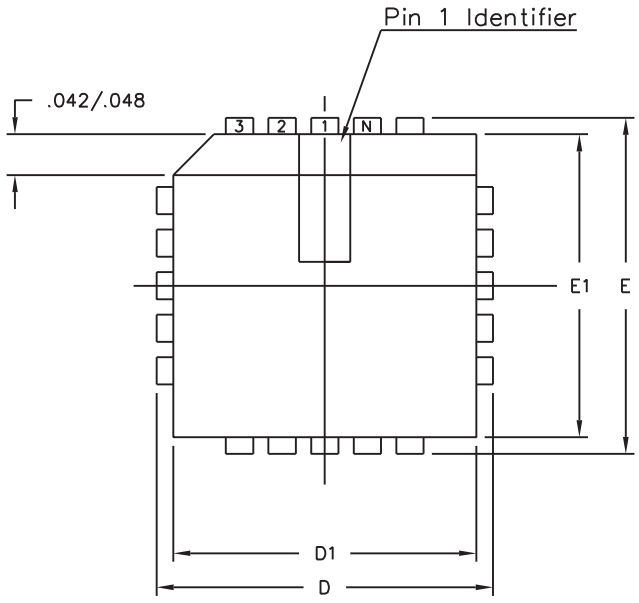

**Figure 3 - Control Memory Timing Diagram**

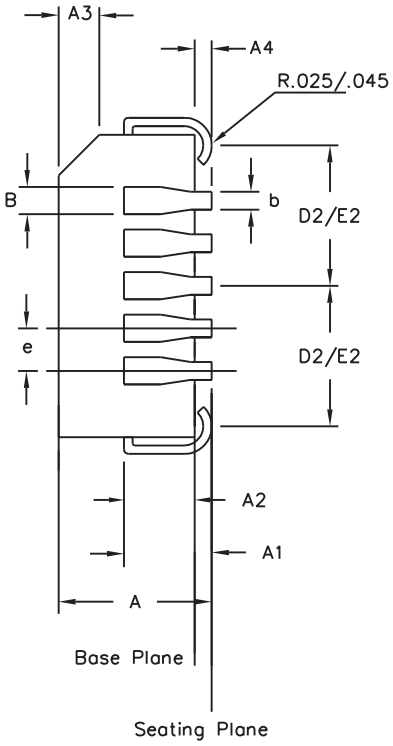
* See Appendix, Fig. A.7 for switching waveform

| AX0 | AX1 | AX2 | AX3 | AY0 | AY1 | AY2 | Connection |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X0-Y0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | X1-Y0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | X2-Y0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | X3-Y0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | X4-Y0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | X5-Y0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | No Connection ① |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | No Connection ① |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | X6-Y0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | X7-Y0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | X8-Y0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | X9-Y0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | X10-Y0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | X11-Y0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | No Connection ① |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | No Connection ① |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | X0-Y1 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | X11-Y1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | X0-Y2 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | X11-Y2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | X0-Y3 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | X11-Y3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | X0-Y4 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | X11-Y4 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | X0-Y5 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | X11-Y5 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | X0-Y6 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | X11-Y6 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | X0-Y7 |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓↓ |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | X11-Y7 |

**Table 1. Address Decode Truth Table**

① This address has no effect on device status.




| Symbol | Control Dir in inch |
|---|---|
| | MIN |
| A | 0.165 |
| A1 | 0.090 |
| A2 | 0.062 |
| A3 | 0.042 |
| A4 | 0.020 |
| D | 0.685 |
| D1 | 0.650 |
| D2 | 0.291 |
| E | 0.685 |
| E1 | 0.650 |
| E2 | 0.291 |
| B | 0.026 |
| b | 0.013 |
| e | 0.050 |
| | |
| ND | |
| NE | |
| N | |
| Note | |
| Conforms to JE | |

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.



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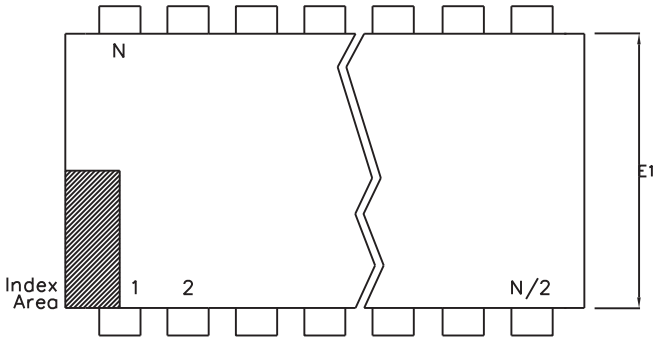
ZARLINK SEMICONDUCTOR

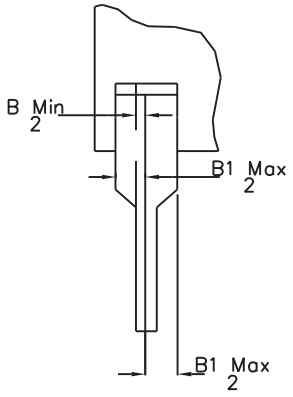
Previous package codes

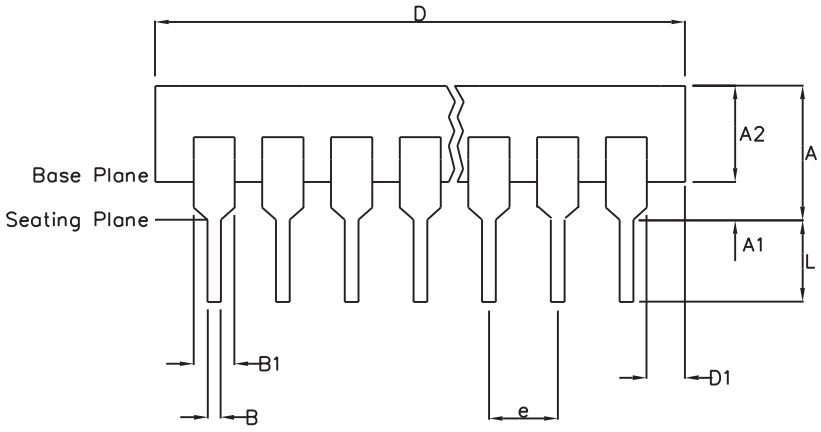
HP / P

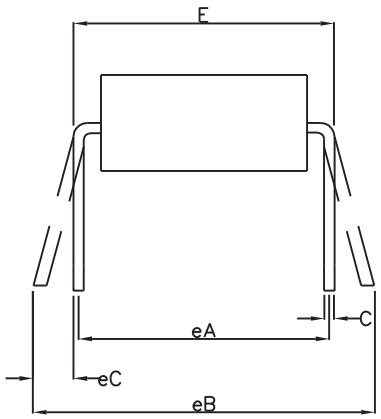
Package

Pack
44 l




| | Min mm |
|---|---|
| A | |
| A1 | 0.3 |
| A2 | 3.1 |
| B | 0.3 |
| B1 | 0.7 |
| C | 0.2 |
| D | 50.2 |
| D1 | 0.1 |
| E | 15.2 |
| E1 | 12.3 |
| e | 2.5 |
| eA | 15. |
| eB | |
| L | 2.9 |
| N | |
| Conforms t | |

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.



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ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package

Pac
40

C

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