muRata Electrical Double Layer Capacitor (EDLC) Technical note

(DMF, DMT/ version 9 / 1st October 2014)

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1. **Principle and structure of EDLC**

1.1. **Principle of EDLC**

Unlike ceramic capacitors or aluminum electrolytic capacitors, Electrical Double Layer Capacitors (EDLC) contain no conventional dielectric. Instead, an electrolyte (solid or liquid) is filled between two electrodes (Fig. 2). In EDLC, an electrical state called “electrical double layer”, which is a pair of electrons and positive ions or a pair of holes and negative ions formed between the electrode and the electrolyte, works as a dielectric and gives capacitance.

Capacitance is proportional to the surface area of electrode. Therefore using activated carbon, which has quite large surface area for electrodes, enables EDLC to have quite high capacitance. The mechanism of ion absorption and desorption to/from the electrode surface contributes to charge and discharge of EDLC. By applying voltage to the facing electrodes, ions are drawn to the surface of the electrode and EDLC is charged (Fig. 2). Conversely, they move away when discharging EDLC. This is how EDLC is charged and discharged.

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**Fig. 1** Principle of electrical double layer capacitor (EDLC)

**Fig. 2** Charge/discharge state in EDLC
1.2. Structure of muRata’s EDLC

In general EDLCs consist of positive electrode, negative electrode, electrolyte and separator which prevents facing electrodes from contacting each other. Activated carbon powder is applied to electricity collector (aluminum foil) of the electrodes (Fig. 1).

The structure of muRata’s EDLC is shown in Fig. 3, Fig. 4 and Fig. 5. Package is made from aluminum laminate film. Aluminum can protect inner materials (multilayered electrodes, electrolyte and so on) from outside circumstance (moisture and so on). Laminate film is coated by insulating plastic layer on surfaces of inner side and outer side for protection from short circuit.

Inner coating resin has also a function of sealing package. EDLC is sealed around four sides by heat-sealing process. Extracting leads are also sealed by same process.

EDLC has two assemblies of unit multilayered-electrode in one package. Partition insulating film is placed between the two of unit cell. An electrode sheet is consisted of electricity collector and activated carbon layer. Activated carbon is printed on surface of electricity collector. Such multiple electrode sheets are layered with mechanically and electrically separated by separator (Fig. 5).

Fig. 3 Structure of muRata’s EDLC (LT cross section)

Fig. 4 Structure of muRata’s EDLC (WT cross section)
1.3. Equivalent circuit model of muRata’s EDLC

Capacitor can be generally described by combination of a capacitor (C), a series resistance (R_s) and an insulation resistance (R_i). muRata’s EDLC has two of unit cell (unit capacitor) which are connected in series in one package therefore simple equivalent circuit model is described like Fig. 6. This simple model having two unit cells can be combined to a simpler model like Fig. 7. In this case, total capacitance value is equal to half of that in unit cell and resistances are equal to two times of that in unit cell.

However such simple model does not generally reflect actual electrical behaviors in EDLCs. This is because that activated-carbon electrode has various-size pores on the surface. Charges are stored by ions moving to the porous surface as mentioned in section 1.1(Fig. 2). Ions can move easily and quickly in the shallow site of electrode. On the other hand, ions move very slowly in the deep site by physical resistance. This means that the shallow site can be fully-charged quickly but full charge at the deep site takes very long time (Fig. 8). From this reason, detailed equivalent model is described with multiple parallel C and multiple series R like Fig. 8.
2. Features of muRata’s EDLCs and your benefits

2.1. Key features and your benefits

muRata’s EDLCs have high capacitance value from some hundreds millifarads to one farad and high rated voltage from 4.2 V to 5.5 V which are suitable for assistance of various batteries and high energy storage (Fig. 9).

EDLCs typically have higher energy density than other capacitors and higher power density than various batteries (Fig. 10). Especially power densities of muRata’s EDLCs are higher than other conventional EDLCs (Fig. 11) and they can discharge up to 100 W. For this reason, muRata’s ones are suitable for high-peak load leveling, high-peak power function, high-power backup or storage for energy harvest.

The thicknesses are very thin, approx. 3.2 mm to 3.7 mm, therefore they can be embedded into various compact and slim devices. Another feature of muRata’s EDLCs is the highest reliability among EDLCs in the market. Because our good package prevents degradation from outside moisture (section 2.4).
Fig. 9 High capacitance of muRata’s EDLCs

Fig. 10 Comparison of power density and energy density

Fig. 11 Comparison with conventional EDLCs
2.2. High energy

muRata’s EDLCs have high energy in a slim package. For example, muRata’s 4.2 V 470 mF EDLC has 2,000 mJ even after 5 years passed under 50°C (* 1). Such energy is 100 times of high-capacitance tantalum capacitor (6.3 V, 1,500 μF) or 12 times of high-cap aluminum capacitor (16 V, 2,200 μF) (Fig. 13). You can design higher energy or reduce space for energy components in your product by using such high-energy-density muRata’s EDLCs.

* 1 EDLCs degrade little by little. Therefore the performance keeps gradually decreasing during long-term use (details in section 6.3). Prediction of performance after degradation is discussed in section 8.1.

2.3. High power

muRata’s EDLCs have high power in a slim package. Lithium coin batteries (Li·MnO₂), lithium thionyl chloride batteries (Li·SOCl₂) etc are being used widely into long-life devices. However those batteries have only quite low power (Fig. 14). In this reason, devices with those batteries are limited to low power function. And although alkaline battery has higher energy than those batteries, it will have shorter life...
time by high-power load. muRata's EDLCs can assist those batteries for high-power function or long-time working with their quite higher power (Fig. 14).

![Graph showing power comparison with various batteries](image)

**30 – 100,000 times of Power vs. batteries**

![Comparison of moisture and sealant effect](image)

**Fig. 14 Power comparison with various batteries**

2.4. High reliability

In general EDLCs have aging which is caused by moisture from outside. And they have also dry up failure. muRata’s EDLCs were improved in aging and dry up.

Moisture is entering into package via sealant part. muRata’s EDLCs are designed its sealant part to be small in order to inhibit moisture (Fig. 15). So there is little damage by moisture compared with cylindrical EDLC that have large damage (Fig. 16). This smallest-designed sealant can also prevent evaporation of electrolyte which causes dry up failure (Details in section 6.2).

![Comparison of moisture and sealant effect](image)

**Fig. 15 Good package for high reliability (against outside use and dry up of electrolyte)**
3. EDLC solutions in your devices

3.1. High peak load leveling

When you have a problem about lack of battery power, muRata’s EDLC can assist it. Boosted power can be gained by connecting EDLC to your battery in parallel (Fig. 17). There is a benefit to improve quality of your product. For example it can improve RF transmission distance to be long, bass sound quality and so on.

If your battery voltage is over EDLC’s rated voltage 4.2 V, you can use a few EDLC in series connection (This is discussed in section 9.2). Please ask muRata if you have a question.

3.2. High peak power function

When you have a problem about quite high peak power in your product, muRata’s EDLC can support it. muRata’s EDLCs can discharge up to some tens ampere for such peak load. EDLC is charged from power source in advance. And then when high power load happens, EDLC discharge to load (Fig. 18). There is a
benefit that new high power function can be added to your product. For example, high brightness LED flash can be added to smart phone, high peak motor function can be added with low power battery.

If your battery voltage is over EDLC’s rated voltage 4.2 V, you can use a few EDLC in series connection (This is discussed in section 9.2). Please ask muRata if you have a question.

### High Peak Power Function

When you need quite high power which power source cannot provide, EDLC can support it. You can add high-power function to your product.

- LED flash
- Motor

![Fig. 18 EDLC for high peak power function](image)

#### 3.3. High-power backup

When you have problems about lack of backup energy in your system, muRata’s EDLC can assist it. EDLC is placed between power source and load in parallel. EDLC is charged by power source all the time. When power interruption happens, EDLC can discharge to load (Fig. 19). There is a benefit to gain high-power and long-time backup in your product. For example, SSD can have high-power and long-life backup into slim devices, portable devices can keep working during battery replacement.

If voltage of power source is over EDLC’s rated voltage 4.2 V, you can use a few EDLC in series connection (This is discussed in section 9.2). Please ask muRata if you have a question.

### High-power Back up

When you need backup energy in case of unexpected shutdown of power source, EDLC can support it. You can design large-energy and high-power backup into slim and small devices.

- Data Backup (SSD, etc...)
- Last Gasp

![Fig. 19 EDLC for high-power back up](image)
3.4. Storage for energy harvest

Energy harvest systems have unstable power generation from solar power, wind energy, thermal energy and so on. muRata’s EDLCs can be charged and discharged easily. Therefore they are suitable for energy storage for unstable power generation. EDLC is placed between harvester and load. If EDLC is charged enough, it can provide stable power to load (Fig. 20).

Fig. 20 EDLC for storage of energy harvesting

4. Lineup of muRata’s EDLC

4.1. Standard EDLCs; DMF series

DMF series is a standard type for versatile applications. DMF has a feature of ultra high power performance up to 100 W discharge (up to 40 W even at -40°C) that other conventional EDLCs do not have. Two products are in the lineup, one is 470 mF and another is 1,000 mF (Table 1). The thickness is 3.2 mm to 3.7 mm that can realize mounting on surface of a circuit board (not reflowable). Therefore these can fit slim products. DMF has also excellent reliability (small aging and excellent durability to dry up failure) in comparison with other EDLCs in the market.

<table>
<thead>
<tr>
<th>P/N</th>
<th>Rated Voltage</th>
<th>Capacitance</th>
<th>Max ESR (1 kHz)</th>
<th>Dimensions (Max)</th>
<th>Operating temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMF3Z5R9H474M3DTA0</td>
<td>Peak 5.5V Constant 4.2V</td>
<td>470 mF ±20%</td>
<td>55 mΩ</td>
<td>14 x 21 x 3.2 mm</td>
<td>-40°C to 70°C</td>
</tr>
<tr>
<td>DMF4B5R5G105M3DTA0</td>
<td>Peak 5.5V Constant 4.2V</td>
<td>1,000 mF ±20%</td>
<td>50 mΩ</td>
<td>14 x 30 x 3.7 mm</td>
<td>-40°C to 70°C</td>
</tr>
</tbody>
</table>

Table 1 Line up of standard EDLC; DMF series
4.2. SSD-specific EDLC; DMT series

DMT series is SSD-specific type that is specially designed for Solid State Drives (SSDs) application. DMT can be used at higher temperature condition up to 85°C compared with DMF series. It has high power performance up to 10W discharge per one piece. One product is in the lineup at this moment. The capacitance is 470 mF and the thickness is 3.5 mm (Table 2) that can realize mounting on surface of a circuit board (not reflowable). DMT has also excellent reliability (small aging and excellent durability to dry up failure) in comparison with other EDLCs in the market.

<table>
<thead>
<tr>
<th>P/N</th>
<th>Rated Voltage</th>
<th>Capacitance</th>
<th>Max ESR (1 kHz)</th>
<th>Dimensions (Max)</th>
<th>Operating temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMT334R2S474M3DTA0</td>
<td>4.2V</td>
<td>470 mF ±20%</td>
<td>150 mΩ</td>
<td>14 x 21 x 3.5 mm</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

Table 2 Line up of SSD-specific EDLC; DMT series

5. Performance of muRata’s EDLCs

5.1. Constant current discharge

When EDLC discharges in constant current condition, voltage on EDLC drops almost linearly with time passing (Fig. 21).

There is an initial voltage drop at the moment of discharge by internal resistance (ESR) in EDLC (ΔV ≈ I*ESR). Initial voltage drop becomes larger in higher current condition. Or it becomes larger also in high ESR EDLC.

After the initial drop, voltage of EDLC drops with time passing. The drop speed depends on current level and nominal capacitance value (ΔV/Δt ≈ I/C). The higher current is or the lower capacitance is, the more quickly voltage drops. However this relation of ΔV/Δt ≈ I/C is equal in ideal state (see left picture in Fig. 8). In case of quite high current discharge or quite low current discharge, the drop speed becomes out of the relation because EDLCs have complex circuit of multiple parallel C (see right picture in Fig. 8).

Fig. 22 and Fig. 23 are actual behaviors in muRata’s EDLCs in constant current discharge. More than 10 A current can be actually discharged from EDLC.
5.2. Constant power discharge

When EDLC discharges in constant power condition, voltage on EDLC drops with time passing (Fig. 24).

There is an initial voltage drop at the moment of discharge by internal resistance (ESR) in EDLC \(\Delta V \approx \frac{I \cdot ESR}{C}\).
P*ESR/Vc). Initial voltage drop becomes larger in higher power condition. Or it becomes larger also in high ESR EDLC.

After the initial drop, voltage of EDLC drops with time passing. The drop speed depends on discharge power, nominal capacitance value and voltage level at the moment (\(dv/dt = P/CV\)). The higher power is or the lower capacitance is, the more quickly voltage drops. In addition, the drop speed becomes higher in lower voltage level with time passing (Fig. 24). However this relation of \(dv/dt = P/CV\) is equal in ideal state (see left picture in Fig. 8). In case of quite high power discharge or quite low power discharge, the drop speed becomes out of the relation because EDLCs have complex circuit of multiple parallel C (see right picture in Fig. 8).

Fig. 25 and Fig. 26 are actual behaviors of muRata’s EDLCs in constant power discharge. More than 10 W power can be discharged from EDLC.

\[
\Delta V \approx i \cdot \frac{P \cdot ESR}{Vc} \\
\frac{dv}{dt} = \frac{-i}{C} = -\frac{P}{CV_i} \\
\frac{dv}{dt} = \frac{-i}{C} = -\frac{P}{CV_2}
\]

Fig. 24 Constant power discharge in EDLC

![Fig. 24 Constant power discharge in EDLC](image)

Fig. 25 Constant power discharge of DMF3Z5R5H474M3DTA0 (discharge from 5.5 V @25°C)
5.3 Temperature dependence in capacitance, ESR and thickness

muRata’s EDLCs have temperature dependence in capacitance, ESR and thickness (Fig. 27, Fig. 28).
DMF3Z5R5H474M3DTA0 has almost no change in capacitance at temperature range from -40°C to 70°C. ESR becomes higher at lower temperature and ESR at -40°C is 2.5 times of one at 25°C. This dependence is caused by temperature dependence in viscous resistance of electrolyte. Thickness becomes larger at higher temperature than room temperature and it get slightly thicker approx. 0.25 mm at 70°C.

In case of DMT334R2S474M3DTA0, capacitance becomes lower at lower temperature. It is 70% at -40°C compared with 25°C capacitance. This is because that DMT has higher inner resistances especially at lower temperature and ions at deeper site are not easy to be charged (Fig. 8). It means that 100% electrical charges cannot be discharged at low temperature. ESR changes with temperature. It becomes higher at lower temperature and ESR at -40°C is 9 times of one at 25°C. This dependence is caused by temperature dependence in viscous resistance of electrolyte. Thickness does not change much even at both of lower temperature and high temperature.
5.4. Charge current and leakage current

EDLCs have characteristic behaviors in current during charging. Fig. 29 and Fig. 30 show charge current behaviors in an ideal capacitor and in an EDLC each other.

In case of an ideal capacitor, charge current will decrease rapidly with time passing and it will get fully-charged in a short time. After fully charged, leakage current will remain (Fig. 29).

However EDLC actually has a lot of various-size pores in electrodes and a complex equivalent circuit model as mentioned in section 1.3 (Fig. 8, Fig. 30). Combination of multiple parallel C and series R contributes to characteristic charge-current. Shallow site of electrode generally has low C and low R therefore high current will flow for quite short time. In contrast, deep site has high C and high R therefore trickle current will keep flowing for quite long time. From those reasons, EDLC takes quite long time to be fully charged and low charge-current trickles for long time.

For lots of application, it is no need to consider such trickle charge-current, however when EDLC is used for applications that have low charge power like energy harvester, it should be considered.

Fig. 31 and Fig. 32 show charge-current behavior of actual muRata’s EDLCs. Trickle current can be observed for hundreds hours. Real leakage current can be considered as less than 1 uA.

\[
\begin{align*}
    i &= i_e \exp \left( -\frac{t}{C \cdot R_i} \right) = \frac{V}{R_s} \exp \left( -\frac{t}{C \cdot R_i} \right) \\
    \ln i &= -\frac{1}{C \cdot R_i} t + \ln \frac{V}{R_s}
\end{align*}
\]

C: capacitance
R_s: series resistance
R_i: Insulation resistance (>>R_s)

Fig. 29 Charge current in an ideal capacitor
Fig. 30 Charge current in an EDLC

\[ i = i_1 + i_2 + \ldots + i_n \]

\[ \ln I_i = \frac{1}{C_s} \left( R_s + R_{s1} + R_{s2} + \ldots + R_{sn} \right) t + \ln \left( \frac{V}{R_s + R_{s1} + R_{s2} + \ldots + R_{sn}} \right) \]

\[ \ln I_a = \frac{1}{C_i \sum R_a} t + a \]

C: capacitance
Rs: series resistance
Ri: insulation resistance

Fig. 31 Charge current of DMF3Z5R5H474M3DTA0 (5.5 V 25°C, n=10)

Fig. 32 Charge current of DMT334R2S474M3DTA0 (4.2 V 25°C, n=10)
6. Reliability of muRata’s EDLCs (Failure and degradation)

6.1. Failure and degradation

There are dry up failure and aging degradation in muRata’s EDLCs.

Dry up failure is caused by gradual evaporation of inside electrolyte to outside during long term use. This failure is open mode. Aging degradation is caused by electrochemical reaction between inner moisture and electrolyte.

6.2. Dry up failure

Dry up is caused by evaporation of inner electrolyte to outside. Such evaporation occurs little by little for long time. Electrolyte has limited minimum amount for EDLC to work well. If there is enough amount of electrolyte inside over minimum value, there is no effect to EDLC performance. At the moment the amount of electrolyte becomes under limited minimum value by evaporation, shortage of ions occurs and available electrode area becomes smaller. As a result, capacitance becomes lower rapidly, ESR becomes larger rapidly and EDLC cannot work in the end (Fig. 33). Dry up failure is open mode.

muRata’s EDLCs are designed to have extra amount of electrolyte in order to expand dry up life time. And also the package is designed to prevent dry up (Fig. 15). Evaporation speed depends on temperature condition, in other words, dry up life time also depends on it. Please refer indication of Fig. 34 for considering how long time EDLC can work. However limited operating time should be also considered (see section 7.2).

![Fig. 33 Capacitance and ESR change by dry up](image-url)
6.3. Aging degradation

Aging is caused by electrochemical reaction between inner moisture and electrolyte. Such electrochemical reaction makes product on surface of electrode. Such product causes performance degradation (capacitance decrease and ESR increase, Fig. 35). Moisture enter inside from outside little by little, therefore the degradation occurs little by little (Fig. 35), not sudden death. Electrochemical reaction amount depends on temperature and voltage, and moisture entering depends on temperature, therefore aging speed depends on temperature and voltage.

muRata’s EDLCs are designed to reduce aging speed by selecting good materials and designing good package (Fig. 36).
6.4. How to consider reliability

There are aging degradation and dry up failure in using EDLC as explained above. However those two are actually not mixed and there is only aging mode until dry up starts (Fig. 37). Therefore only aging mode should be considered if dry up lifetime is expected to be long enough.

Fig. 36 Good package design for reducing dry up (evaporation of electrolyte)

6.5. Examples of reliability test (DMF test for 9,000 hours at 4.2 V 50°C and DMT test for 7,000 hours at 4.2 V 70°C)

Fig. 38 and Fig. 39 show the results of test at 4.2 V 40°C for 9,000 hours to DMF3Z5R5H474M3DTA0 and 4.2 V 70°C for 7,000 hours to DMT334R2S474M3DTA0. The aging degradation can be observed in them. Although such degradation is large at first, it converges gradually.
Fig. 38 Capacitance and ESR change in test at 4.2 V 40°C for 9,000 hours to DMF3Z5R5H474M3DTA0

Fig. 39 Capacitance and ESR change in test at 4.2 V 70°C for 7,000 hours to DMT334R2S474M3DTA0

7. Cautions for use

Cautions in using EDLC are mentioned in this section. However please make sure to check the cautions in the specification sheet of each product before using.

7.1. Limitation to applications

Please contact us before using our products for the applications listed below which require especially high reliability for the prevention of defects which might directly cause damage to the third party’s life, body or property.

(1) Aircraft equipment, (2) Aerospace equipment, (3) Undersea equipment, (4) Power plant control equipment, (5) Medical equipment, (6) Transportation equipment (vehicles, trains, ships, etc.), (7) Traffic signal equipment, (8) Disaster prevention / crime prevention equipment, (9) Data-processing equipment, (10) Application of similar complexity and/or reliability requirements to the applications listed in the above.

Please do not use this product for any applications related to military equipment.
7.2. Limited operating time

Each product has specific limited operating time to get failure which depends on use condition. Fig. 40 and Fig. 41 show the limited operating time in DMF3Z5R5H474M3DTA0 and DMT334R2S474M3DTA0 each other.

In case of DMF3Z5R5H474M3DTA0 (Fig. 40), if it is used at continuous 5.5 V charge, limited operating time is 500 hours at 70°C, 3,200 hours at 50°C and 6,400 hours at 40°C. In using at less than 4.2 V, 3,000 hours at 70°C, 20,000 hours at 50°C and 40,000 hours at 40°C. If voltage or temperature is intermittent, the time will be longer.

In case of DMT334R2S474M3DTA0 (Fig. 41), voltage level does not effect the time. The limited operating time is 9,000 hours at 85°C, 40,000 hours at 70°C and more than 300,000 hours at 40°C. If temperature is intermittent, the time will be longer.

Fig. 40 Use condition and limited operating time of DMF3Z5R5H474M3DTA0
7.3. Voltage

7.3.1. Polarity and applicable wave form

Please verify the orientation of EDLC and use in correct polarity in accordance with the markings on the products. In principle, EDLC has no polarity. However if the inverse voltage is impressed EDLC, significant degradation of capacitance or leakage of electrolyte may be possibly caused. From this reason, please use with the permitted loading and do not use with the restricted loading shown in Fig. 42.

Fig. 42 Permitted loading and restricted loading

7.3.2. Withstand voltage of EDLCs

Please ensure not to apply excessive voltage over the specific rated voltage between positive and negative terminals. Applying higher voltage on EDLC may cause significant degradation, electrolyte
leakage or swelling.

7.3.3. Voltage balance

muRata’s EDLCs have two unit cells connected in series per one products (Fig. 43). Please be sure to control voltage balance between each cell with using balance terminal for the following two purposes:

1) To prevent each cell from being applied excessive voltage that may cause significant degradation.

2) To prevent shortening of the life time: By making capacitor voltage equal, variation in the rate of degradation can be controlled. It allows long-term use of EDLCs.

For more details, please see section 10.

Fig. 43 muRata’s EDLCs have two capacitors in series into one package

7.4. Temperature and self heating

Please use EDLCs under less than the specific operating temperature with considering not only circumstance temperature but also self heating of EDLCs. For reference, please see section 12.2.

7.5. Soldering and assembling

Reflow and flow soldering cannot be accepted because body temperature of EDLC will get higher than allowable maximum temperature. Please use other mounting methods like hand iron soldering, auto iron soldering, connector and so on.

Please do not apply excessive force to the capacitor during insertion as well as after soldering. The excessive force may result in damage to electrode terminals and/or degradation of electrical performance.

Recommendation of iron soldering is discussed in section 11.

Please do not wash the device after soldering.

8. Simulation of performance in your use condition through life

8.1. Simulation of performance and degradation

Please note that EDLC’s performance will decrease gradually. It depends on your use condition (impressed voltage to EDLC and surround temperature). For your design, muRata has simulation tools that can calculate Cap/ESR degradation and discharge performance at end of your set life in given condition (Fig. 44).

This calculation is based on the acceleration factors of voltage and temperature. Such acceleration
factors were gained from several actual acceleration tests. Please contact us for details of performance in your condition.

Simulation tools, available in any conditions.

[use-condition parameters]
- Charge voltage to EDLC
- Surround temperature
- Expected life time
- Discharge current or power
- Minimum working voltage you can accept
- P/N of EDLC
- Connection number of EDLCs (series or/and parallel)

[Simulation output]
- Capacitance/ESR degradation in your condition (voltage per cell and temperature)
- EDLC discharge behavior (voltage vs time) in initial and end of your set life

Fig. 44 Simulation tool for performance in any condition of muRata’s EDLCs

8.2. Examples of capacitance and ESR degradation in various conditions

Several examples of estimated capacitance and ESR degradation in various conditions are shown in this section. They are the times at which capacitance reaches 75% of the initial value and ESR reached 2 times of the initial values (Fig. 45).
8.2.1. Examples of DMF series

Estimated time at which capacitance reaches 75% of the initial value and ESR reached 2 times of the initial value related to DMF series are shown in Table 3 and Table 4. The conditions are 3.0 V to 5.5 V at 20 °C to 40 °C.

### Table 3 Times at which capacitance reaches 75% of the initial value about DMF series

<table>
<thead>
<tr>
<th>DMF series</th>
<th>20 °C</th>
<th>30 °C</th>
<th>40 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V</td>
<td>180,000 hours (20 years)</td>
<td>90,000 hours (10 years)</td>
<td>45,000 hours (5 years)</td>
</tr>
<tr>
<td>3.6 V</td>
<td>130,000 hours (15 years)</td>
<td>90,000 hours (10 years)</td>
<td>45,000 hours (5 years)</td>
</tr>
<tr>
<td>4.2 V</td>
<td>35,000 hours (4 years)</td>
<td>22,000 hours (2.5 years)</td>
<td>13,000 hours (1.5 years)</td>
</tr>
<tr>
<td>5.0 V</td>
<td>17,000 hours (2 years)</td>
<td>9,000 hours (1 year)</td>
<td>5,000 hours (0.6 years)</td>
</tr>
<tr>
<td>5.5 V</td>
<td>10,000 hours (1.2 years)</td>
<td>6,000 hours (0.7 years)</td>
<td>3,500 hours (0.4 years)</td>
</tr>
</tbody>
</table>

### Table 4 Times at which ESR reaches 2 times of the initial value about DMF series

<table>
<thead>
<tr>
<th>DMF series</th>
<th>20 °C</th>
<th>30 °C</th>
<th>40 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V</td>
<td>180,000 hours (20 years)</td>
<td>90,000 hours (10 years)</td>
<td>45,000 hours (5 years)</td>
</tr>
<tr>
<td>3.6 V</td>
<td>180,000 hours (20 years)</td>
<td>90,000 hours (10 years)</td>
<td>45,000 hours (5 years)</td>
</tr>
<tr>
<td>4.2 V</td>
<td>180,000 hours (20 years)</td>
<td>90,000 hours (10 years)</td>
<td>45,000 hours (5 years)</td>
</tr>
<tr>
<td>5.0 V</td>
<td>70,000 hours (8 years)</td>
<td>38,000 hours (4.5 years)</td>
<td>22,000 hours (2.5 years)</td>
</tr>
<tr>
<td>5.5 V</td>
<td>40,000 hours (4.5 years)</td>
<td>23,000 hours (2.5 years)</td>
<td>13,000 hours (1.5 years)</td>
</tr>
</tbody>
</table>
8.2.2. Examples of DMT series

Estimated time at which capacitance reaches 75% of the initial value and ESR reached 2 times of the initial value related to DMT series are shown in Table 5 and Table 6. The conditions are 3.0 V to 4.2 V at 40 °C to 80 °C.

<table>
<thead>
<tr>
<th>DMT series</th>
<th>40 °C</th>
<th>50 °C</th>
<th>70 °C</th>
<th>80 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V</td>
<td>27,000 hrs</td>
<td>18,000 hrs</td>
<td>8,000 hrs</td>
<td>5,500 hrs</td>
</tr>
<tr>
<td>3.6 V</td>
<td>17,000 hrs</td>
<td>11,000 hrs</td>
<td>5,000 hrs</td>
<td>3,500 hrs</td>
</tr>
<tr>
<td>4.2 V</td>
<td>12,000 hrs</td>
<td>8,000 hrs</td>
<td>3,500 hrs</td>
<td>2,500 hrs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DMT series</th>
<th>40 °C</th>
<th>50 °C</th>
<th>70 °C</th>
<th>80 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 V</td>
<td>&gt;180,000 hrs</td>
<td>&gt;180,000 hrs</td>
<td>60,000 hrs</td>
<td>32,000 hrs</td>
</tr>
<tr>
<td>3.6 V</td>
<td>&gt;180,000 hrs</td>
<td>160,000 hrs</td>
<td>46,000 hrs</td>
<td>25,000 hrs</td>
</tr>
<tr>
<td>4.2 V</td>
<td>&gt;180,000 hrs</td>
<td>130,000 hrs</td>
<td>37,000 hrs</td>
<td>20,000 hrs</td>
</tr>
</tbody>
</table>

9. For increasing capacitance, energy, power or voltage

9.1. Solution of parallel connection of EDLCs

When higher energy and/or higher power are required in your system, you can get it by connecting some EDLCs in parallel (Fig. 46). If N pcs of EDLCs are connected in parallel, total capacitance becomes high to N times and total ESR becomes low to 1/N. You can get both of higher energy (calculated from E=1/2*C*V^2) and higher power. In parallel connection case, it is possible to connect different parts of EDLCs.

Please design balance circuit in any connection (described in section 10).

Fig. 46 Parallel connection of EDLCs

9.2. Solution of series connection of EDLCs

When higher voltage is required to EDLC in your system, you can get it by connecting some EDLCs in series. For example, in case that battery voltage is over the rated voltage 4.2 V of EDLC, the voltage to EDLC should be reduced by buck convertor or some EDLCs should be connected in series (Fig. 47). And
also when you require higher energy, you can get it by boosting voltage to EDLC with some EDLCs connected in series.

Please note that in case of N pcs connection in series, total capacitance becomes low to 1/N and total ESR becomes high to N times. However you would get higher energy (calculated from $E=\frac{1}{2}C*V^2$).

Additionally series connection has also an effect to reduce degradation of EDLC through long term. Such degradation depends on voltage, therefore it is possible to reduce it by derating the impressed voltage per one EDLC.

In case of series connection, please do not pair any different part (different capacitance, different series, new/old, and so on). Please pair EDLCs of completely same part number.

If n pcs of EDLCs are connected in series, the acceptable voltage of EDLC will be n times of the rated voltage.

Please design balance circuit in any connection (described in section 10).

![Series connection of EDLCs](image)

**Fig. 47 Series connection of EDLCs**

### 10. Balance circuit for long time use

muRata’s EDLCs are consisted of two of capacitor unit cell in series for increasing voltage (Fig. 48). For example, DMF3Z5R5H474M3DTA0 (470mF) has two of 940mF cell in series. Therefore there is a possibility that each voltage that is impressed to each capacitor may be unbalanced due to variation of each capacitance or insulated resistance. When such unbalance occurs during using EDLC, impressed voltage to one cell will be high. If the voltage exceeds the limited value, it causes large electrical degradation. And difference of impressed voltage may also cause difference of life time between each cells.
as a result it may reduce life time of EDLC product.

For balance of such voltages, EDLCs need to have balance control of each impressed voltages. There are two methods, one is passive balance control and another is active balance control.

![Passive balance control](image)

**Fig. 48** muRata’s EDLCs have two capacitors in series into one package

10.1. **Passive balance control**

Passive balance control is consisted of resistances (Fig. 49). This is a simple and low cost solution. The resistance value should be decided with considering load pattern or current value. The lower resistance is, the faster balance convergence is. However power loss consumed through resistances becomes higher in using lower resistances (Table 7). Such power consumption loss will keep continuously even after voltage convergence.

For your choice, please choose resistance value within the range of your acceptable power consumption. Also please don’t exceed the limited maximum value as shown (Table 8).

![Passive balance circuit](image)

**Fig. 49** Passive balance circuit
Table 7 Balance resistance value and balance current/power consumption

<table>
<thead>
<tr>
<th>Resistance value</th>
<th>Maximum balance current</th>
<th>Convergence speed</th>
<th>Power consumption through resistances</th>
<th>Circuit loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>1kΩ</td>
<td>4.2 mA</td>
<td>Faster</td>
<td>8.82 mW</td>
<td>Higher</td>
</tr>
<tr>
<td>10kΩ</td>
<td>420 uA</td>
<td>↑</td>
<td>882 uW</td>
<td>↑</td>
</tr>
<tr>
<td>100kΩ</td>
<td>42 uA</td>
<td>↓</td>
<td>88.2 uW</td>
<td></td>
</tr>
<tr>
<td>1MΩ</td>
<td>4.2 uA</td>
<td></td>
<td>8.82 uW</td>
<td>Lower</td>
</tr>
<tr>
<td>10MΩ</td>
<td>420 nA</td>
<td></td>
<td>882 nW</td>
<td>Lower</td>
</tr>
</tbody>
</table>

(note) Values in chart is in case of 4.2 V impressed to EDLC products.

(Reference) Insulated resistance of EDLC is over 1Mohm.

Table 8 Maximum resistance value

<table>
<thead>
<tr>
<th>Impressed Voltage between + and -</th>
<th>Max. Balance Resistance value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P/N</td>
<td>DMF3Z5R5H474M3DTA0</td>
</tr>
<tr>
<td>~2.7V</td>
<td>No need balance</td>
</tr>
<tr>
<td>~3.0V</td>
<td>4.7 MΩ</td>
</tr>
<tr>
<td>~3.2V</td>
<td>2.2 MΩ</td>
</tr>
<tr>
<td>~3.6V</td>
<td>1.0 MΩ</td>
</tr>
<tr>
<td>~4.0V</td>
<td>470 kΩ</td>
</tr>
<tr>
<td>~4.2V</td>
<td>220 kΩ</td>
</tr>
<tr>
<td>~4.5V</td>
<td>47 kΩ</td>
</tr>
<tr>
<td>~5.0V</td>
<td>4.7 kΩ</td>
</tr>
<tr>
<td>Over 5.0V</td>
<td>1.0 kΩ</td>
</tr>
</tbody>
</table>

10.2. Active balance control

Active balance control is a circuit with using operational amplifier (Fig. 50). This can have faster convergence of voltage balance by current amplification function even if high resistances are used.

The rated voltage of operational amplifier should be higher than Vcc. Damping resistor may be needed in order to avoid abnormal oscillation. Operational amplifier should be chosen with considering power consumption and drive current (Table 9).

Active balance circuit works only in condition of voltage unbalance. After voltage balance converged, there is only power consumption of no load. Therefore Active balance is excellent in energy efficiency. Operational amplifier with high slew rate has high speed motion and an advantage for short-time balance.
convergence. However such high-speed amplifier has high power consumption (Table 9). It should be chosen with considering your purpose.

Fig. 50 Active balance circuit

![Active balance circuit diagram](image)

**Table 9 Operational amplifier properties**

<table>
<thead>
<tr>
<th>Indication for choice</th>
<th>General Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew rate</td>
<td>Low ←→ High</td>
</tr>
<tr>
<td>Drive current</td>
<td>Low ←→ High</td>
</tr>
<tr>
<td>Power consumption</td>
<td>Low ←→ High</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Narrow ←→ Wide</td>
</tr>
<tr>
<td>Application</td>
<td>Wide use ←→ Particular use</td>
</tr>
<tr>
<td>Cost</td>
<td>Low ←→ High</td>
</tr>
</tbody>
</table>

10.3. Comparison between passive balance and active balance

Table 10 shows comparison between passive balance and active balance. Passive balance method has advantages of small mount area or low cost. On the other hand, active balance method has advantages of high-speed balance convergence and low power consumption. Please choose balance method with considering function and cost.
Table 10 Comparison of passive and active balance

<table>
<thead>
<tr>
<th>Type</th>
<th>Passive balance (using resistance)</th>
<th>Active balance (using OPAMP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mount area</td>
<td>Small</td>
<td>Middle to Large</td>
</tr>
<tr>
<td>Circuit cost</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Power consumption</td>
<td>High</td>
<td>Middle to low</td>
</tr>
<tr>
<td>Convergence speed</td>
<td>Slow</td>
<td>Fast</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>No limit</td>
<td>Limited</td>
</tr>
</tbody>
</table>

11. Solder mounting method

muRata’s EDLC DMF/DMT series should be mounted by hand soldering. Please make pretreatment of your PCB in advance. The procedure is described below (Fig. 51).

1. Please put the solder paste on the land.
2. Please melt solder paste by reflow process (*2) and form solder layer on the land.
3. Please temporarily fix the EDLC on the PCB by a double-stick tape or something.

![Fig. 51 Process of pretreatment](image)

After the pretreatment, please solder EDLC by hand. The procedure is described below (Fig. 52). Choose step 1-2-4 or step 1-3-4. There is a video tutorial for soldering. Please ask us for it.

1. Please heat both of EDLC terminal and PCB land by soldering iron and melt a solder on the land.
2. Please put the pre-cut length of solder wire (for Φ1mm, 2-3mm length) on a terminal (*4) and heat until it melts (*3).
3. Please put solder wire on a terminal and heat until it melts (*3).
* 2 The condition of reflow profile depends on solder materials. Please confirm it with the vendor of solder paste. For reference, please see the following example of the reflow profile (Fig. 53).

* 3 There is limited time for heating. It is 3.0 (+1/0) seconds per one terminal (Fig. 54). Allowable soldering frequencies are 3 times per one EDLC. Please do not touch laminate package directly by solder iron.

* 4 Please be careful not to break the terminals by pulling them by tweezers because those aluminum part is breakable.
12. Safety of muRata’s EDLCs

12.1. Case of short circuit by any possibility

Even if charged EDLC is externally short-circuited by any possibility, there are no leakage of electrolyte, no smoke, no ignition or no rupture. The reason is because of low energy inside unlike batteries. DMF or DMT has just only 5 to 10 joules of energy. Such energy is just equal to only 1°C to 2°C temperature increase of 1 g water. Therefore there is little heated in case of short.

For your information, when DMF3Z5R5H474M3DTA0 charged in 5.5 V is short-circuited, 120 A current will be flowed for a very short time (Fig. 55). Maximum current depends on internal resistance.

12.2. Heat generation during use

When you use EDLCs, please note heat generation during charge/discharge. Such heat generation may be very low and it is no problem in many situations because of very low energy in EDLCs. However in
In case of high power and high frequency use, heat generation could be high as explained below.

Heating depends on consumption energy during charge or discharge of EDLC. EDLC has very lower energy than battery. For example, 4V 3,000 mAh battery has approximately 40 kJ energy, on the other hand DMF35Z55H474M3DTA0 (5.5V 470mF) or DMT334R2S474M3DTA0 (4.2V 470mF) has only approximately 4 J to 7 J energy (E=1/2*CV^2). Therefore heat generation during charge or discharge will be very low. At a rough estimate, those muRata’s EDLCs have approximately 1 J/K heat capacity, therefore even if all the energy is instantly discharged (short circuit case), temperature will possibly increase less than 10°C. And such temperature increase is momentary and it will decrease quickly by heat radiation.

However if charge/discharge cycle is repeated frequently, heat may be possibly accumulated into EDLC and increased temperature may keep continuously. It depends on current, frequency and duty ratio. It is related with balance between heat generation and heat radiation (Fig. 56).

Fig. 57 is an example of actual heat generation of EDLC. If 5A 30ms peak current is repeated per second to DMF-008TEMP (5.5V 1,000mF), temperature increases gradually. And it converges at 3°C increase after 300 seconds. This converging status means that heating generation is equal to heat radiation.

![Fig. 56 Heat generation and heat radiation](image-url)
Fig. 57 Example of actual heat generation